

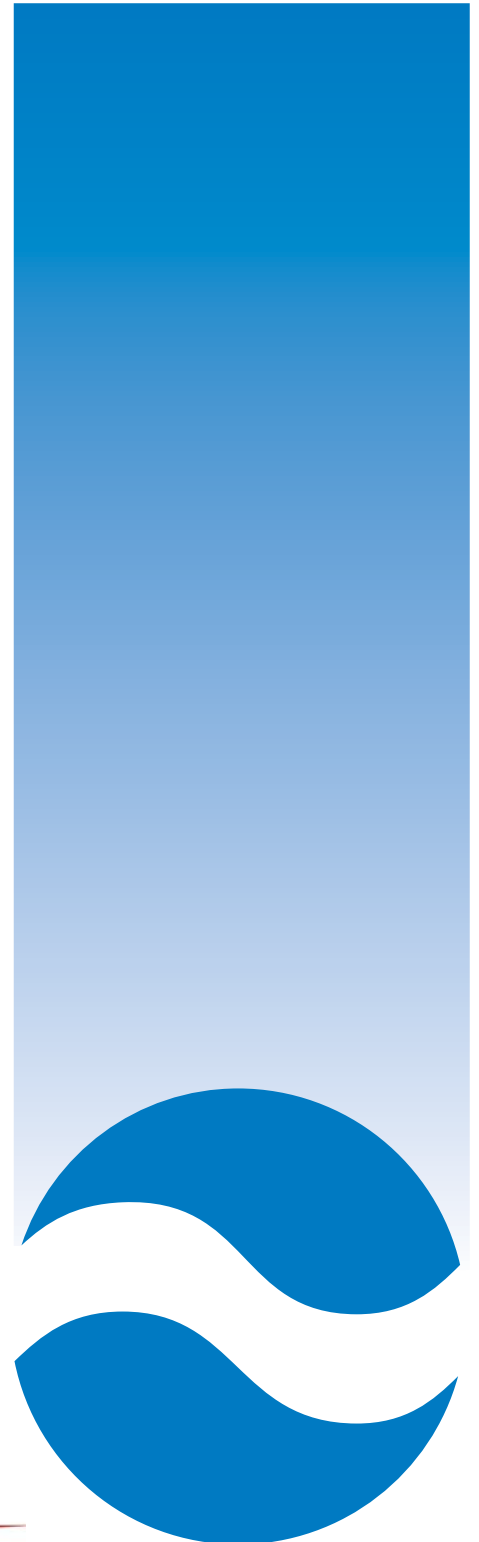
EIA/IPC/JEDEC J-STD-002D

June 2013

Supersedes J-STD-002C  
w/Amendment 1  
December 2008

# **JOINT INDUSTRY STANDARD**

Solderability Tests for  
Component Leads,  
Terminations, Lugs,  
Terminals and Wires



---

**Notice**

ECIA, IPC and JEDEC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of ECIA, IPC or JEDEC from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than ECIA, IPC or JEDEC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by ECIA, IPC or JEDEC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, ECIA, IPC or JEDEC do not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement. The material in this joint standard was developed by the IPC Components and Wire Solderability Specification Task Group (5-23b) of the Assembly and Joining Processes Committee (5-20), the Electronic Components Industry Association Soldering Technology Committee (STC) and the JEDEC Solid State Technology Association Committee (JC14.1)

*For Technical Information Contact:*

**EIA Standards  
Electronic Components  
Industry Association**

2214 Rock Hill Rd, Suite 170  
Herndon, VA 20170-4212  
Phone: (571) 323-0294  
Fax: (571) 323-0245

**IPC  
Association Connecting  
Electronics Industries®**

3000 Lakeside Drive, Suite 309S  
Bannockburn, IL 60015-1249  
Phone: (847) 615-7100  
Fax: (847) 615-7105

**JEDEC Solid State Technology  
Association**

3103 North 10th Street, Suite 240-S  
Arlington, VA 22201-2107  
Phone: (703) 907-7540  
Fax: (703) 907-7583

Please use the Standard Improvement Form shown at the end of this document.



EIA/IPC/JEDEC J-STD-002D

# Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

A joint standard developed by IPC Components and Wire Solderability Specification Task Group (5-23b) of the Assembly and Joining Processes Committee (5-20), the Electronic Components Industry Association Soldering Technology Committee (STC) and the JEDEC Solid State Technology Association Committee (JC14.1)

Users of this standard are encouraged to participate in the development of future revisions.

#### Contact:

**EIA Standards  
Electronic Components  
Industry Association**

2214 Rock Hill Road, Suite 170  
Herndon, VA 20170-4212  
Phone: (571) 323-0294  
Fax: (571) 323-0245

**JEDEC Solid State Technology  
Association**

3103 North 10th Street, Suite 240-S  
Arlington, VA 22201-2107  
Phone: (703) 907-7540  
Fax: (703) 907-7583

**IPC  
Association Connecting  
Electronics Industries®**

3000 Lakeside Drive, Suite 309S  
Bannockburn, IL 60015-1249  
Phone: (847) 615-7100  
Fax: (847) 615-7105

#### **Supersedes:**

J-STD-002C w/Amendment 1 -  
November 2008  
J-STD-002C - December 2007  
Amendment 1 - October 2008  
J-STD-002B - February 2003  
J-STD-002A - October 1998  
J-STD-002 - April 1992

This Page Intentionally Left Blank

## Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Components and Wire Solderability Specification Task Group (5-23b) of the Assembly and Joining Processes Committee (5-20) are shown below, it is not possible to include all of those we assisted in the evolution of this joint industry standard. Additionally, there were many participants from the Electronic Components Industry Association Soldering Technology Committee (STC) and the JEDEC JC-14.1 Reliability Test Methods for Packaged Devices. To each of them, the members and staffs of IPC, ECIA and JEDEC Associations extend their gratitude.

---

### IPC Assembly & Joining Processes Committee

Chair  
Leo P. Lambert  
EPTAC Corporation

Vice Chair  
Renee J. Michalkiewicz  
Trace Laboratories - Baltimore

### IPC Component & Wire Solderability Specification Task Group

Chair  
David D. Hillman  
Rockwell Collins

Vice Chair  
Dennis Fritz  
MacDermid, Inc.

### EIA Soldering Technology Committee

Chair  
Douglas W. Romm  
Texas Instruments Inc.

### JEDEC JC14.1 Reliability Test Methods for Packaged Devices

Chair  
Ife Hsu  
Intel Corporation

---

### IPC Component & Wire Solderability Specification Task Group

Ross Dillman, ACI/EMPF  
Constantino Gonzalez, ACME Training & Consulting  
Neil Witkowski, Alcatel-Lucent  
Bradley Smith, Allegro MicroSystems Inc.  
Karen Tellefsen, Alpha  
Andrew Giamis, Andrew Corporation  
George Wenger, Andrew Corporation  
Greg Alexander, Ascentech, LLC  
Fritz Byle, Astronautics Corp. of America  
Jeffery Kukelhan, BAE Systems Platform Solutions  
Marvin Banks, Ball Aerospace & Technologies  
Gerald Leslie Bogert, Bechtel Plant Machinery, Inc.  
Robert Wettermann, BEST Inc.  
Beverley Christian, BlackBerry  
Thomas Carroll, Boeing Company  
Michael Paddack, Boeing Company  
Mary Bellon, Boeing Research & Development

Michael Jawitz, Boeing Research & Development  
Todd MacFadden, Bose Corporation  
Jason Bragg, Celestica  
Prakash Kapadia, Celestica  
Louis Hart, Compunetics Inc.  
Mark Fulcher, Continental Automotive Systems  
Brian Madsen, Continental Automotive Systems  
Jose Servin, Continental Temic SA de CV  
David Corbett, Defense Supply Center Columbus  
Robert Heber, Defense Supply Center Columbus  
Lowell Sherman, Defense Supply Center Columbus  
Glenn Dody, Dody Consulting  
Michael Toben, Dow Electronic Materials  
Anne Lomonte, Draeger Medical Systems, Inc.  
Peter Bratin, ECI Technology, Inc.  
Michael Pavlov, ECI Technology, Inc.

Karl Wengenroth, Enthone Inc.  
Yung-Herng Yau, Enthone Inc.  
Leo Lambert, EPTAC Corporation  
Thomas Carlstrom, Ericsson AB  
Gerald Gagnon, Exttech Instruments Corporation  
John Thompson, FCI USA, Inc.  
Harjinder Ladhar, Flextronics  
Terry Munson, Foresite, Inc.  
Paco Solis, Foresite, Inc.  
Martin Bayes, Four Square Consulting  
Michael Yuen, Foxconn CMMMSG-NVPD  
Graham Naisbitt, Gen3 Systems Limited  
Brian Wardhaugh, Gen3 Systems Limited  
Gregg Klawson, General Dynamics - C4 Systems  
Donald Gerstle, Google  
Brian Toleno, Henkel Corporation  
Richard Davidson, Honeywell Aerospace

Suzanne Nachbor, Honeywell  
Aerospace Minneapolis

Vicka White, Honeywell Inc. Air  
Transport Systems

Fujiang Sun, Huawei Technologies  
Co., Ltd.

Yunhua (Danny) Tu, Huawei  
Technologies Co., Ltd.

James Bielick, IBM Corporation

James Maguire, Intel Corporation

Mark Kwoka, Intersil Corporation

Reza Ghaffarian, Jet Propulsion  
Laboratory

J. Lee Parker, JLP

David Scheiner, Kester

David Lober, Kyzen Corporation

Todd Jarman, L-3 Communications

Roger Su, L-3 Communications

Vijay Kumar, Lockheed Martin  
Missile & Fire Control

Linda Woody, Lockheed Martin  
Missile & Fire Control

Hue Green, Lockheed Martin Space  
Systems Company

Dennis Fritz, MacDermid, Inc.

Francis Anglade, Metronelec

Laya (Yan) Chen, Microtek  
(Changzhou) Laboratories

Russell Shepherd, Microtek  
Laboratories Anaheim

Edwin Bradley, Motorola Solutions,  
Inc.

Christopher Hunt, National Physical  
Laboratory

Keith Sweatman, Nihon Superior Co.,  
Ltd.

Kil-Won Moon, NIST

Maureen Williams, NIST

Darrell Freiwald, Northrop Grumman

Mahendra Gandhi, Northrop  
Grumman Aerospace Systems

Joseph Sherfick, NSWC Crane

Richard Kraszewski, Plexus Corp.

Carol Handwerker, Purdue University

Bill Bear, Raytheon Company

Richard Iodice, Raytheon Company

Jeff Seekatz, Raytheon Company

Jeff Shubrooks, Raytheon Company

Royce Taylor, Raytheon Company

Bill Vuono, Raytheon Company

Lance Brack, Raytheon Missile  
Systems

Robert Morris, Raytheon Missile  
Systems

Martin Scionti, Raytheon Missile  
Systems

William Russell, Raytheon  
Professional Services LLC

Steven Herrberg, Raytheon Systems  
Company

Christian Klein, Robert Bosch GmbH

Jason Koch, Robisan Laboratory Inc.

Chris Mahanna, Robisan Laboratory  
Inc.

David Adams, Rockwell Collins

DeAnn Gibbs, Rockwell Collins

Rachel Grinvalds, Rockwell Collins

David Hillman, Rockwell Collins

Eddie Hofer, Rockwell Collins

Gaston Hidalgo, Samsung  
Telecommunications America

Henry Rekers, Schneider Electric

Giovanni Casanova, Schweitzer  
Engineering Laboratories, Inc.

Donald Abbott, Sensata Technologies

Gerard O'Brien, Solderability Testing  
& Solutions, Inc.

Stephen Meeks, St. Jude Medical

Mel Parrish, STI Electronics, Inc.

Christine Blair, STMicroelectronics  
Inc.

William Sepp, Technic Inc.

Richard Edgar, Tec-Line Inc.

Douglas Romm, Texas Instruments  
Inc.

Shirley He, The 5th Electronic  
Institute of MII

Elizabeth Allison, Trace Laboratories  
- Baltimore

Renee Michalkiewicz, Trace  
Laboratories - Baltimore

Debora Obitz, Trace Laboratories -  
Baltimore

John Radman, Trace Laboratories -  
Denver

Calette Chamness, U.S. Army  
Aviation & Missile Command

Jere Wittig, Unknown Address

George Milad, Uyemura International  
Corp.

Chris Ball, Valeo Inc.

Dale Albright, Winslow Automation  
aka Six Sigma

Russell Winslow, Winslow  
Automation aka Six Sigma

Theodore Edwards

John Rohlfing

# Table of Contents

<b>1</b>	<b>PREFACE</b>	1	4.2.1	Test A - SnPb Solder – Solder Bath/Dip and Look Test (Leads, Wires, etc.)	7
1.1	Scope	1	4.2.2	Test B - SnPb Solder – Solder Bath/Dip and Look Test (Leadless Components)	9
1.2	Purpose	1	4.2.3	Test C - SnPb Solder – Wrapped Wires Test (Lugs, Tabs, Terminals, Large Stranded Wires)	10
1.2.1	Shall and Should	1	4.2.4	Test D - SnPb or Pb-free Solder – Resistance to Dissolution of Metallization Test	12
1.3	Method Classification	1	4.2.5	Test S - SnPb Solder – Surface Mount Process Simulation Test	13
1.3.1	Visual Acceptance Criteria Tests	1	4.2.6	Test A1 - Pb-free Solder – Solder Bath/Dip and Look Test (Leads, Wires, etc.)	14
1.3.2	Force Measurement Tests	1	4.2.7	Test B1 - Pb-free Solder – Solder Bath/Dip and Look Test (Leadless Components)	15
1.4	Coating Durability	2	4.2.8	Test C1 - Pb-free Solder – Wrapped Wires Test (Lugs, Tabs, Terminals, Large Stranded Wires)	16
1.5	Solderability Backwards Compatibility	2	4.2.9	Test S1 - Pb-free Solder – Surface Mount Process Simulation Test	17
1.6	Referee Verification Solder Dip for Tests A, B, C, A1, B1, and C1	2	4.3	Force Measurement Tests	19
1.7	Limitations	2	4.3.1	Test E - SnPb Solder – Wetting Balance Solder Pot Test (Leaded Components)	19
1.8	Contractual Agreement	2	4.3.2	Test F - SnPb Solder – Wetting Balance	20
1.9	Terms and Definitions	2	4.3.3	Test G - SnPb Solder – Wetting Balance Globule Test	22
<b>2</b>	<b>APPLICABLE DOCUMENTS</b>	3	4.3.4	Test E1 - Pb-free Solder – Wetting Balance Solder Pot Test (Leaded Components)	24
2.1	Industry	3	4.3.5	Test F1 - Pb-free Solder – Wetting Balance Solder Pot Test (Leadless Components)	25
2.1.1	IPC	3	4.3.6	Test G1 - Pb-free Solder – Wetting Balance Globule Test	26
2.1.2	International Electrotechnical Commission	3	<b>5</b>	<b>NOTES</b>	27
2.2	Government	3	5.1	Use of Activated Flux	27
2.2.1	Federal	3	5.2	Massive Components	27
<b>3</b>	<b>REQUIREMENTS</b>	3	5.3	Sampling Plans	27
3.1	Materials	3	5.4	Correction for Buoyancy	27
3.1.1	Solder	3	5.5	Preconditioning Limitations	28
3.1.2	Flux	3	<b>APPENDIX A</b>	<b>Critical Component Surfaces</b>	29
3.1.3	Standard Copper Wrapping Wires	4	<b>APPENDIX B</b>	<b>Evaluation Aids</b>	38
3.1.4	Water	4	<b>APPENDIX C</b>	<b>Calculation of Maximum Theoretical Force</b>	43
3.2	Equipment	4	<b>APPENDIX D</b>	<b>Calculation of Integrated Value of Area of the Wetting Curve</b>	45
3.2.1	Steam Preconditioning Apparatus	4			
3.2.2	Bake Preconditioning Apparatus	4			
3.2.3	Optical Inspection Equipment	5			
3.2.4	Dipping Equipment	5			
3.2.5	Timing Equipment	5			
3.3	Preparation for Testing	5			
3.3.1	Specimen Preparation and Surface Condition	5			
3.3.2	Steam Conditioning	6			
3.3.3	Surfaces to be Tested	6			
3.4	Solder Bath Requirements	6			
3.4.1	Solder Contamination Control	6			
<b>4</b>	<b>TEST PROCEDURES</b>	7			
4.1	Application of Flux	7			
4.2	Visual Acceptance Criteria Tests	7			

<b>APPENDIX E</b>	<b>Informative Annex</b> .....	46	Figure A-10	Through-Hole Components - Round Pin	37
<b>APPENDIX F</b>	<b>J-STD-002/J-STD-003 Activated Solderability Test Flux Rationale Committee Letter</b> .....	47	Figure B-1	Defect Size Aid	38
<b>APPENDIX G</b>	<b>Graphical Representations: Progression of Solder Wetting Curve Parameters As Measured By Wetting Balance Testing</b> .....	49	Figure B-2	Types of Solderability Defects	39
			Figure B-3	Aids in Evaluation of 5% Allowable Area of Pin Holes	40
			Figure B-4	Aid in Evaluation of 5% Allowable Area of Pin Holes	41
<b>APPENDIX H</b>	<b>Test Protocol for Wetting Balance Gauge Repeatability and Reproducibility (GR&amp;R) Using Copper Foil Coupons</b> .....	52	Figure B-5	Solderability Coverage Guide	42
			Figure C-1	Lead Periphery and Volume for a 132 I/O PQFP	43

### Figures

Figure 3-1	Example Reticle	5
Figure 4-1	Dipping Schematic	8
Figure 4-2	Solder Dipping Angle for Surface Mount Leaded Components	8
Figure 4-3	Solder Dipping Depth for Through-Hole Components	9
Figure 4-4	Leadless Component Immersion Depth	10
Figure 4-5	Illustration of Acceptable Solderable Terminal	11
Figure 4-6	Illustration of Unsolderable Terminal	11
Figure 4-7	Illustration of Acceptable Solderable Stranded Wire	11
Figure 4-8	Illustration of Partially Solderable Stranded Wire Showing Incomplete Fillet	11
Figure 4-9	Wetting Balance Apparatus	19
Figure 4-10	Set A Wetting Curve	21
Figure 4-11	Set B Wetting Curve	21
Figure 4-12	Component and Dipping Angle (Directly from IEC 60068-2-69)	24
Figure A-1	“J” Leaded Components	29
Figure A-2	Passive Components	30
Figure A-3	Gull Wing Components	31
Figure A-4	Leadless Chip Carrier	32
Figure A-5	“L” Leaded Component	33
Figure A-6	Exposed Pad Package	34
Figure A-7	Bottom-Only Termination Component	34
Figure A-8	Area Array Component Critical Surface	35
Figure A-9	Through-Hole Components - Flat Pin	36

### Tables

Table 3-1	Flux Compositions	4
Table 3-2	Steam Temperature Requirements	5
Table 3-3	Preconditioning Parameters for Solderability Testing	6
Table 3-4	Maximum Limits of Solder Bath Contaminant	7
Table 4-1	Test A Solderability Testing Parameters	8
Table 4-2	Test B Solderability Testing Parameters	10
Table 4-3	Test C Solderability Testing Parameters	11
Table 4-4	Test D Solderability Testing Parameters	13
Table 4-5	Stencil Thickness Requirements	13
Table 4-6	Reflow Parameter Requirements	14
Table 4-7	Test S Solderability Testing Parameters	14
Table 4-8	Test A1 Solderability Testing Parameters	15
Table 4-9	Test B1 Solderability Testing Parameters	16
Table 4-10	Test C1 Solderability Testing Parameters	17
Table 4-11	Stencil Thickness Requirements	18
Table 4-12	Pb-free Reflow Parameter Requirements	18
Table 4-13	Test S1 Solderability Testing Parameters	18
Table 4-14	Wetting Balance Parameter and Suggested Evaluation Criteria	20
Table 4-15	Dipping Angle and Immersion Depth for Components (Directly from IEC 60068-2-69)	23
Table 4-16	Wetting Parameters and Suggested Evaluation Criteria	24
Table 3-1	Flux Compositions	47

# Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

---

## 1 PREFACE

**1.1 Scope** This standard prescribes test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wires, stranded wires, lugs, and tabs. This standard also includes a test method for the resistance to dissolution/dewetting of metallization. This standard is intended for use by both vendor and user.

**1.2 Purpose** Solderability evaluations are made to verify that the solderability of component leads and terminations meets the requirements established in this standard and to determine that storage has had no adverse effect on the ability to solder components to an interconnecting substrate. Determination of solderability can be made at the time of manufacture, at receipt of the components by the user, or just before assembly and soldering.

The resistance to dissolution of metallization determination is made to verify that metallized terminations will remain intact throughout the assembly soldering processes.

*In the case of a discrepancy, the description or written criteria always takes precedence over the illustrations.*

**1.2.1 Shall and Should** The words “shall” or “shall not” are used in the text of this document wherever there is a requirement for materials, preparation, process control, or acceptance of a soldered connection or a test method. The word “should” reflects recommendations and is used to reflect general industry practices and procedures for guidance only.

Other documents to extent specified by the customer.

**1.3 Method Classification** This standard describes methods by which component leads or terminations may be evaluated for solderability. Any one of the following test methods - Test A, Test B, Test C, Test D, and Test S - may be used for SnPb solder processes and any one of the following test methods - Test A1, Test B1, Test C1, Test D, and Test S1 - may be used for Pb-free solder processes and are to be used for each application as a default unless otherwise AABUS.

### 1.3.1 Visual Acceptance Criteria Tests

Test A – Solder Bath/Dip and Look Test (Leaded Components and Stranded Wires) SnPb Solder (4.2.1)

Test B – Solder Bath/Dip and Look Test (Leadless Components) SnPb Solder (4.2.2)

Test C – Wrapped Wires Test (Lugs, Tabs, Hooked Leads, and Turrets) SnPb Solder (4.2.3)

Test D – Resistance to Dissolution/Dewetting of Metallization Test SnPb Solder and Pb-free Solder (4.2.4)

Test S – Surface Mount Process Simulation Test SnPb Solder (4.2.5)

Test A1 – Solder Bath/Dip and Look Test (Leaded Components and Stranded Wires) Pb-free Solder (4.2.6)

Test B1 – Solder Bath/Dip and Look Test (Leadless Components) Pb-free Solder (4.2.7)

Test C1 – Wrapped Wires Test (Lugs, Tabs, Hooked Leads, and Turrets) Pb-free Solder (4.2.8)

Test S1 – Surface Mount Process Simulation Test Pb-free Solder (4.2.9)

### 1.3.2 Force Measurement Tests

Test E – Wetting Balance Solder Pot Test (Leaded Components) SnPb Solder (4.3.1)

Test F – Wetting Balance Solder Pot Test (Leadless Components) SnPb Solder (4.3.2)

Test G – Wetting Balance Globule Test SnPb Solder (4.3.3)

Test E1 – Wetting Balance Solder Pot Test (Leaded Components) Pb-free Solder (4.3.4)

Test F1 – Wetting Balance Solder Pot Test (Leadless Components) Pb-free Solder (4.3.5)

Test G1 – Wetting Balance Globule Test Pb-free Solder (4.3.6)