IPC/JEDEC-9706

2013 - December

Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

A standard developed by IPC

Association Connecting Electronics Industries

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.

©Copyright 2013. IPC, Bannockburn, Illinois. All rights reserved under both international and Pan-American copyright conventions. *Any copying, scanning or other reproduction of these materials without the prior written consent of the copyright holder is strictly prohibited and constitutes infringement under the Copyright Law of the United States.*

IPC/JEDEC-9706

Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

Developed by the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1) and the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product Reliability Committee (6-10) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Members of the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1) and the SMT Attachment Reliability Test Methods Task Group (6-10d) of the IPC Product Reliability Committee (6-10) have worked together to develop this document. We would like to thank them for their dedication to this effort. Any document involving a complex technology draws material from a vast number of sources. While the principal members of the SMT Attachment Reliability Test Methods Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of JEDEC and IPC extend their gratitude.

Product Reliability Committee

Chair
Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory

Vice Chair
James Monarchio
TTM Technologies, Inc.

JC-14.1 JEDEC Reliability Test Methods for Packaged Devices Committee

Chair
Ife Hsu
Intel Corporation

6-10d SMT Attachment Reliability Test Methods Task Group

Chair
Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory

Vice Chair
Vasu Vasudevan
Intel Corporation

6-10d SMT Attachment Reliability Test Methods Task Group

Neil Adams, Circuit Check Inc.

Mudasir Ahmad, Cisco Systems Inc.

Aileen Allen, Hewlett-Packard Company

Michael Azarian, University of Maryland

Elizabeth E. Benedetto, Hewlett-Packard Company

Trevor S. Bowers, Adtran Inc.

Nicole Butel, Avago Technologies

Beverley Christian, BlackBerry

Harold Ellison, Quantum Corporation

Dennis Fritz, MacDermid, Inc.

Enrico Galbiati, GEST Labs S.r.l. a Socio Unico

David D. Hillman, Rockwell Collins

Christopher Hunt, National Physical Laboratory

Jeffrey C.B. Lee, Integrated Service Technology - ISTi

Anna Lifton, Alpha

Anne Lomonte, Draeger Medical Systems, Inc.

Alan McAllister, Intel Corporation

James J. Monarchio, TTM Technologies, Inc.

Jim Mulvey, Lockheed Martin Space Systems Company

David Nelson, Raytheon Company

Keith G. Newman, Hewlett-Packard Company

Satish Parupalli, Intel Corporation

Jagadeesh Radhakrishnan, Intel Corporation

John M. Radman, Trace Laboratories - Denver

Gnyaneshwar Ramakrishna, Cisco Systems Inc.

Paul Reid, PWB Interconnect Solutions Inc.

Russell S. Shepherd, Microtek Laboratories Anaheim

Julie Silk, Agilent Technologies

Ramgopal Uppalapati, Intel Corporation

Wesley M. Wolverton, Raytheon Systems Company

Andy Zhang, Texas Instruments

A special note of thanks goes to Ramgopal Uppalapati, Mike H. Williams, and Sanjay Goyal of Intel Corparation for coordinating the development of this document.

Table of Contents

1 **SCOPE** 1

1.1 Purpose 1

1.2 Background 1

1.3 Performance Classification 1

1.4 Definition of Terms 1

1.4.1 FCBGA package 1

1.4.2 SMT 1

1.4.3 Product Component 1

1.4.4 Voltage Metrology 1

1.4.5 Power Ball 1

1.4.6 Safe xyz... 2

1.4.7 Ball-level Fault Isolation 2

1.4.8 Signal Ball 2

1.4.9 Daisy-chain 2

1.4.10 TH 2

1.4.11 G 2

1.4.12 α-error 2

1.4.13 β-error 2

1.4.14 TV 2

1.4.15. Event detector 2

1.4.16. USL 2

1.4.17. FPGA 2

1.5 Interpretation “Shall” 2

2 **APPLICABLE DOCUMENTS** 2

2.1 IPC 2

2.2 JEDEC 2

2.3 Joint Industry Standard 2

3 **SAMPLE SIZE** 2

4 **APPARATUS AND SET UP** 3

4.1 Voltage Metrology Introduction 3

4.2 Voltage Metrology 3

4.3 Lab Set-up Description 4

4.3.1 Test Board with FCBGA Component of Interest 4

4.3.2 Electrical Monitoring Device/Equipment and Software 5

4.3.3 Peripherals 5

5 **FAILURE DISPLAY AND CRITERION** 5

6 **DATA ANALYSIS GUIDELINES** 5

7 **FAILURE ANALYSIS** 5

8 **REFERENCES** 5

Appendix A In-situ Metrology Case Study — Voltage Metrology Based Lab Set-up Illustration 6

A.1 Component FCBGA 6

A.2 Test Board 6

A.3 Plug Connector 6

A.4 Ribbon Cables 6

A.5 Receptacle Connectors 7

A.6 Interface Box

A.7 Voltage Measuring Device 8

A.8 Assembly/Set-up 8

A.9 Failure Display and Criteria 8

Appendix B Voltage In-situ Metrology Validation Results 10

B.1 Component-level Test with no Thermal Solution Compression Load 10

B.2 System-level Test with FCBGA Thermal Solution Compression Load 11

Appendix C Connector Validation Case Study Results 13

Appendix D Hand-probe False Failure Rate compared to Shock Voltage In-situ Detection Metrology 14

Appendix E Voltage Metrology Measurement Capability Analysis Study Results 15

Figures

Figure 4-1 Schematic Illustrating the Concept behind the Voltage Metrology 3

Figure 4-2 Schematic Illustrating Application of Voltage Metrology on Daisy Chain Test Vehicles 3

Figure 4-3 Schematic illustrating Package side Connections (dotted lines) to Enable Ball by Ball Fault Isolation on Daisy-chained Test Vehicles 4

Figure 4-4 Generic Shock In-situ Metrology Test Set-up 4

Figure A-1 Board Routing to Enable Voltage Metrology on a Product Package 6

Figure A-2 A 2x7 pin Connector Soldered to a 14 Pin Header on the Board 6

Figure A-3 Illustration of a 14 Wire Ribbon Cable 7

Figure A-4 Illustration Showing 2 x 7 Female Connector 7

Figure A-5 Illustration Showing Interface Box 7

Figure A-6 Shock In-Situ Metrology Test Set-up 8

Figure A-7 Failure Display during a Shock Test using Voltage Metrology 9

Figure B-1 Test Board Design and Monitored Corner Balls (in green) and Shock Test Profile used for In-situ Metrology Validation 10

Figure B-2 In-situ Metrology Validation Results under no Thermal Solution enabling Load Condition 11

Figure B-3 Schematic Showing System-level Test PCI Configuration Set-up with Heat Sink enabling on FCBGA Component 11

Figure B-4 In-situ metrology Validation Results under 20lbs Thermal Solution enabling Load Condition 12

Figure B-5 In-situ metrology Validation Results under 60lbs Thermal Solution enabling Load Condition 12

Figure C-1 Picture Showing Test Board Design, Shock Profile, and Connector Validation Results 13

Figure D-1 Results Plot showing Fails that would Have Been Passed after the Test 14

Figure E-1 Measurement Correlation Study Results for one such Voltage-based In-situ Metrology 15

Tables

Table D-1 Hand Probe False Failure Rate 14

Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

1 SCOPE

This document establishes metrology guidelines to electrically and reliably detect solder joint opens on Flip-Chip Ball Grid Array (FCBGA) SMT board assemblies during the mechanical shock or drop event. In-situ metrology can monitor not only FCBGA assembly with daisy-chain components but can also monitor product components with power or ground planes or equivalent daisy-chain test structures. In addition, the metrology is capable of providing ball-level resolution provided appropriate test structures are designed into the test package and board. The metrology was validated for thermal solutions with compression load. Although the initial focus of this metrology is specific to FCBGA assemblies in mechanical shock or drop testing, the same approach can eventually be extended to other stress tests (e.g. vibration, mechanical bend, and temperature cycle) and/or components (including other BGAs, sockets assemblies and TH/SMT leaded/leadless assemblies) depending on evolution and adoption of the guidelines (title and scope could be updated based on the outcome from future planned studies). This metrology may not be capable of detecting partial solder ball cracks, since resistance does not significantly change until the solder crack is close to 100%. Finally, the detection of pad cratering failures will be possible through use of this metrology, provided there is a complete trace crack.

1.1 Purpose This document provides:

- Description of concept behind efficient in-situ electrical metrology to reliably detect FCBGA assembly solder joint opens during mechanical shock or drop test
- Guidelines for special daisy-chain test structure to standardize test board design for ball-level electrical monitoring of FCBGA joints
- Minimum requirements to establish the metrology in the lab for execution
- Definition for in-situ electrical open detection criteria
- Guidelines for electrical and FA data analysis

1.2 Background Some of the existing metrologies, including JESD22-B110, JESD22-B11, and IPC/JEDEC-9703, do not provide in-situ electrical monitoring of FCBGA solder joint opens during test. They either rely on electrical test before and after the test or use less efficient destructive physical analysis techniques which are either not reliable (see Appendix D for false fail rate based on hand probe e-test), cost-effective, or time consuming. The proposed shock metrology provides reliable electrical data with ball-level resolution, thereby eliminating the need for further fault isolation. Finally, the metrology provides instantaneous response in display format, thereby reducing the testing throughput time with minimal to no physical destructive failure analysis needs [1]. Solder joint built-in self-test (SJ BIST) in-situ metrology usage was neither demonstrated on a large scale sample size, nor was it applied on non-field programmable gate array (non-FPGA) packages [2]. Traditional daisy chain resistance measurement is usually limited by a combination of speed and channel count. In addition, the metrology does not provide ball-level resolution or cannot monitor board assemblies with real product components. Current based event detectors are more prone to noise due to poor resolution and no results display (to confirm failures) compared to voltage metrology.

1.3 Performance Classification At this point in time, the reliability requirements need to be established by agreement between customer and supplier and this document only provides guidelines on how to use in-situ test method.

1.4 Definition of Terms The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

1.4.1 FCBGA package: (Flip-chip) ball grid array component (does not include connectors or sockets).

1.4.2 SMT Surface-mount technology.

1.4.3 Product Component Any functional component used in electronic industry that has ground or power planes or equivalent test structures.

1.4.4 Voltage Metrology Name of the new metrology described in this document that can detect electrical failures on product component.

1.4.5 Power Ball Ball on the FCBGA component used for voltage power.