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ESD Association Technical Report

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For ESD Electronic Design Automation Checks

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1.0 PURPOSE

The purpose of this document is to provide a guideline for both EDA industry and ESD design community to establish a comprehensive ESD electronic design automation (EDA) verification flow satisfying the ESD design challenges of modern ICs. This includes the definition of a common terminology and the description of the required check types. The document is also aimed to convey the basic ESD concepts and their implementation during the IC design process to EDA industry.

The document is not limited to specific ESD concepts or EDA solutions of specific vendors, but covers in a generic way typical checks which require a certain EDA tool set and database. Once these tools are available it is the responsibility of an IC design company, integrated device manufacturer (IDM) or foundry to implement the specific rules as part of their particular design and verification flows.

2.0 INTRODUCTION

The verification of ESD protection of a complex IC design with many supply domains and voltage levels, various functional parts (RF, digital, analog) and high voltage circuitry is extremely challenging. Consequently, manual verification of the ESD protection poses significant risks of missing design flaws. Therefore, an automated ESD check - partial or complete - is highly desired in today's design flow.

To address this need, many IC design companies have created in-house tools and flows to perform automated ESD checks. However, most of these tools focus on specific ESD checks and lack comprehensive ESD check functionality [1, 2, 3].

An ideal ESD verification flow should:

- Provide broad check coverage, allow components' verification along the progress of a design, and include ESD checks at all IC design phases (conceptual phase, main design phase and final IC verification) to avoid changes of circuit blocks (to ensure ESD compliance) at the later stages of the design.
- Limit the required manual checks to a minimum.
- Be transparent and seamlessly integrate into the adopted design flow and design rule checking environment.
- Be run directly by IC designers.
- Provide clear and informative descriptions of violations; do not report false positive violations.

This report will describe an ESD EDA verification flow meeting the aforementioned requirements. The structure of the report is as follows:

- Section 3.0 outlines how the different checks described throughout the report correspond to typical IC product and ESD IP development flows. It also highlights design data/information available for use by ESD EDA tools at each product stage.
- Section 4.0 introduces basic ESD concepts.
- Section 5.0 provides an overview of checks to verify that circuits in the design are properly protected from ESD. These checks verify circuits that cannot shunt ESD energy, circuits that are required to shunt all ESD energy, and the ones that are able to shunt a portion of the ESD energy.
- Section 6.0 describes the checks aimed at the verification of the ESD protection network integrations. These checks are performed at cell level, intra-power domain level, inter-power domain level and package level.