ESD TR5.4-03-11

Revision and redesignation of ANSI/ESD SP5.4-2008

ESD Association Technical Report

ESD TR5.4-03-11

For Electrostatic Discharge Sensitivity Testing

Latch-Up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits

Transient Latch-up Testing – Component Level Supply Transient Stimulation

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FOREWORD

This technical report (TR) was originally issued as a standard practice (SP), ANSI/ESD SP5.4. A standard practice is a test method which can be considered a best practice but has not been demonstrated to produce repeatable and reproducible results. Since the writing of the SP, the complexity of integrated circuits has increased and many circuits today require vectors to establish the stable, low current state needed to accurately identify a latch-up condition. Furthermore, other stress surges have been identified in various published experiments which can cause TLU and which are even more severe than the trigger pulses in SP5.4. Since there was no widely available equipment which could both provide the stress pulse required for ANSI/ESD SP5.4 and apply vectors to stabilize the device after the transient latch-up (TLU) stress, further experiments to analyze and improve the TLU testing methodology defined in SP5.4 could not be performed. Additionally the idea of a negative going power supply stress pulse to induce latch-up never caught on. Most engineers involved in latch-up testing now favor a transient stress on I/Os or a positive stress pulse on power supplies for inducing TLU, since these are believed to better match use conditions. For these reasons, WG 5.4 decided not to continue work on the current standard practice document and instead opted to change the SP into a TR. Classifying the document as a TR preserves the work in developing the test procedure, which can still prove useful as a latch-up characterization or diagnostic tool for specific integrated circuits. Allowing the document to stay as a permanent SP was not considered wise since the term standard practice implies a level of acceptability and universality that the test method in its current form will likely never attain.

This document is largely unchanged from ANSI/ESD SP5.4. This forward has been added to explain the change from an SP to a TR, the purpose and scope have been modified, the term “technical report” has been substituted for “standard practice” where appropriate and a number of typographical errors have been corrected. The original annexes included a note that the annexes were not part of ANSI/ESD SP5.4. These notes have been removed since this document is no longer intended to become a standard test method or standard.

This technical report was originally designated ANSI/ESD SP5.4-2004 and approved on February 22, 2004. ANSI/ESD SP5.4-2008 was a reaffirmation of ANSI/ESD SP5.4-2004 and was approved on September 7, 2008. ESD TR5.4-03-11 is a revision and re-designation of ANSI/ESD SP5.4-2008 and was published on October 31, 2011.

At the time the ESD TR5.4-03-11 was prepared, the 5.4 Device Testing (TLU) subcommittee had the following members:

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TABLE OF CONTENTS

ANNEXES

FIGURES

ESD Association Technical Report For Electrostatic Discharge Sensitivity Testing - Latch-Up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits - Transient Latch-up Testing – Component Level - Supply Transient Stimulation

1.0 SCOPE AND PURPOSE

1.1 Purpose

The information and procedures defined in this technical report may be used to search for latch-up sensitive layouts within integrated circuits. The stress levels and stimuli parameter values defined may be used for a wide range of devices. Levels and values can be scaled up or down to suit the requirements of the actual device under test and types of transient stimuli being used.

1.2 Scope

This technical report describes a procedure for measuring latch-up sensitivity of integrated circuits to transients on power supply lines. Circuits on which this test method may be applied include CMOS (Complementary Metal Oxide Semiconductor), Bipolar, and BiCMOS (Bipolar-CMOS) devices typically requiring less than 30 volts for operation. The range of integrated circuits on which this procedure has been shown to be useful is limited.

2.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms, available for complimentary download at www.esda.org.

3.0 PERSONNEL SAFETY

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment should be followed.

4.0 TEST ENVIRONMENT

The criteria for humidity process control and parts handling can be found in ANSI/ESD S20.20. The ambient temperature under which the test is performed must be controlled to 23 °C ± 5 °C. Higher temperatures for the DUT can be used by utilizing temperature forcing/measurement equipment if desired, but control to within ± 5 °C is recommended. Previous experience with the latch up test method JESD 78 (Section 6.11) suggests that higher temperature will result in lower failure thresholds or greater susceptibility to failure. The DUT temperature used for a given test must be recorded and reported.

5.0 DEVICE HANDLING CRITERIA

A process must be established for safely handling ESD sensitive devices to ensure that parts are not subjected to damaging ESD events.