

ANSI/ESDA/JEDEC JS-002-2014

ESDA/JEDEC Joint Standard

ANSI/ESDA/JEDEC JS-002-2014

Revision and Replacement of ANSI/ESD S5.3.1-2009 &
JEDEC JESD22-C101F

*For Electrostatic Discharge
Sensitivity Testing*

*Charged Device Model (CDM) -
Device Level*

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*ESDA/JEDEC Joint Standard for
Electrostatic Discharge Sensitivity Testing -
Charged Device Model (CDM) -
Device Level*

Approved August 29, 2014
ESD Association & JEDEC Solid State Technology Association



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FOREWORD

This joint standard was developed under the guidance of the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a Joint Working Group composed of both ESDA and JEDEC. The new standard is intended to replace the existing Charged Device Model ESD standards (JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards.

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is the human-body model (HBM). However, with the increasing use of automated device handling systems another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM a device itself becomes charged (e.g., by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package may be less susceptible to CDM damage at a given voltage, compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

This joint standard is a first collaborative result of combining the different CDM platform and measurement devices of both ESDA and JEDEC standards into a single platform standard document. It aims to optimize use of test systems currently in the field, while improving the waveform measurement capability in determining calibrated waveform parameters to maintain the JEDEC legacy data for use in today's systems. The key combining principle employed in this joint document is the use of current instead of voltage to define test conditions. While CDM voltages will still be reported, the underlying tester verification method uses discharge currents from the JEDEC calibration modules. This is the critical feature that allows the combination of the two former methods into one while maintaining connection to the vast majority of legacy CDM threshold data. More description of the current-based test condition approach is given in Annex C of the document. During development of this joint standard it was discovered (from waveform measurements using high bandwidth oscilloscopes) that additional ferrites (or other high frequency response modifications to the CDM test head) to meet JEDEC waveform compliance with a 1 GHz oscilloscope were being implemented in existing systems. This resulted in distortion of the actual discharge waveform. This standard now prohibits use of these components. Removal of ferrites in existing test heads or replacement of existing test heads with ferrite free versions, are both straightforward modifications to ensure JS-002 compliance. Additionally, initial CDM tester qualification using a high bandwidth oscilloscope is now required to ensure compliance.

This is a living document and further improvements in hardware, metrology and test procedure based on this platform are anticipated to be described in future revisions.

This standard is maintained and revised as a joint standard through a Memorandum of Understanding between JEDEC and ESDA. This standard is a living document and revisions and updates will be made on a routine basis driven by the needs of the electronic industry.

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ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level**1.0 SCOPE AND PURPOSE****1.1 Scope**

This standard establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. To perform the tests, the devices must be assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This test method combines the main features of JEDEC JESD22-C101 and ANSI/ESD S5.3.1. New verification procedures and test condition definitions have been introduced to facilitate this combination.

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms¹

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices²

JESD88, Dictionary of Terms for Solid-State Technology²

JESD625, Requirements For Handling Electrostatic Discharge-Sensitive (ESDS) Devices²

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)¹

IEC61340-5-1 – Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General Requirements³

3.0 DEFINITIONS

The following definitions are in addition to those found in the ESD Association's Glossary of Terms:

Charged device model electrostatic discharge (CDM-ESD). An electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal.

¹ ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937; FAX: 315-339-6793; www.esda.org

² JEDEC Global Standards for the Microelectronics Industry; www.jedec.org

³ IEC – International Electrotechnical Commission, www.iec.ch