ESD Association Standard Practice

For Electrostatic Discharge Sensitivity Testing –

Near-Field Immunity Scanning - Component/Module/PCB Level

ANSI/ESD SP14.5-2015

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard
Approved September 14, 2015

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Approved August 21, 2015
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FOREWORD

One of the biggest problems when ESD testing a functional system or sub-system is the analysis of unacceptable soft-errors, upsets, bit errors and similar faults that occur during ESD testing. These failures are also referred to as “soft” failures, which are non-destructive and the unit being tested works fine when re-set or re-booted. Following a “soft” failure, no physical evidence exists to allow troubleshooting using traditional methods.

Scanning as described in this document provides a method of identifying areas, traces, and individual devices sensitive to ESD therefore providing engineers with key information to deduce the causes of “soft” failures. Knowing the failure and specific areas sensitive to the ESD event allows the engineer to apply product/circuit knowledge to identify root cause and correct the problem.

This standard practice[1] defines a test method for evaluating the sensitivity of IC’s, modules or boards for susceptibility to field-coupled impulsive disturbances. The main focus lies on soft-errors, i.e., upsets, bit errors etc. The field-coupled disturbance is derived from measured field pulses as they can occur inside a system subjected to human-metal ESD, as it is defined by the IEC 61000-4-2 system level ESD test standard.

The motivation for using near-field immunity scanning is to determine the robustness of IC’s, modules or PCB’s is fivefold:

Localizing sensitive areas. While the system level standard allows one to determine if a system is passing or failing, it does not identify the root cause of an ESD sensitivity. Root-cause analysis is best done with near-field immunity scanning.

Repeatability. The problems of repeatability of system level testing are well publicized and near field scanning has been shown to offer much better reproducibility in determining ESD sensitivities.

Relative characterization at the module level. System level testing requires having a complete, operational system, but using near-field scanning allows one to determine the sensitivity of individual modules against ESD-like pulses.

Relative characterization at the IC level. Many ESD problems, especially in hand-held products, are not caused by coupling into the PCB, but rather by direct coupling into the IC’s. Using a near-field scanning system, one can determine the sensitivity of an IC to electric or magnetic field coupling.

Fulfillment of system level requirements. Using near-field scanning techniques, one can compare the sensitivities of previous and new models, and in many cases obtain good indications of robustness without retesting the complete system. This test method is not a substitute for system-level testing but compliments it by providing a tool for identifying problem areas.

This standard practice was designated ANSI/ESD SP14.5-2015 and approved on August 21, 2015.

[1] **ESD Association Standard Practice (SP):** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it is not reproducible.

At the time ANSI/ESD SP14.5-2015 was prepared, the 14.0 System Level ESD Subcommittee had the following members:

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1.0 PURPOSE AND SCOPE

1.1 Purpose

The purpose of this standard practice is to establish a test method for immunity scanning of ICs, modules and PCB's. Results from scanning *relate* to the system level performance but cannot be used to predict system level performance using the IEC 61000-4-2 test method. The reason is that variations exist in coupling paths between injection points and local current densities and associated fields coupled into traces or IC's.

This standard practice addresses testing of ICs, modules, and PCB's under powered conditions. This test method focuses on soft errors, such as bit errors and upsets, keeping in mind that fast pulses can also cause latch-up. Use of the standard practice will guide the user in the identification of the root causes of electrostatic discharge (ESD) induced soft errors in IC's, modules, and PCB's, for debugging and quality control purposes.

1.2 Scope

This standard practice establishes the procedure for testing and characterizing the sensitivity of IC's, modules, and PCB's against the effect of field-coupled pulses that are generated by ESD type pulses. The field-coupled pulses derived from the fast leading edge of transmission line pulses closely resemble electromagnetic fields as they occur inside a product subjected to human-metal ESD, such as specified by the IEC 61000-4-2. IEC 61000-4-2 is the primary standard for system level ESD test standard.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard practice to the extent specified herein:

IEC 61000-4-2, Electromagnetic Compatibility (EMC) – Part 4.2: Testing and Measurement Techniques – Electrostatic Discharge Immunity[2]

IEC/TR 61967-1-1, Integrated circuits - Measurement of electromagnetic emissions - Part 1-1: General conditions and definitions - Near-field scan data exchange format[2]

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

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[2] International Electrotechnical Commission; 3, rue de Varembé, CH - 1211 GENEVA 20, Switzerland; www.iec.ch