

ESD Association Technical Report

*For Electrostatic Discharge
Sensitivity Testing –*

Charged Board Event (CBE)

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FOREWORD

In early 2009 an increased number of inquiries were received about a certain type of unexplained "component-on-board" failures that resembled ESD at times and EOS at other times. However, these failures could not be duplicated by using any of the existing ESD Models. Further research indicated that these problems were related to the so-called Charged Board Event (CBE), an ESD phenomenon pertaining to the charging up of the boards and creating stress on the components or ICs mounted on them. CBE type of ESD events have been recognized already since 1983, but there is still not commonly agreed methods to classify or analyze CBE cases. Purpose of this Technical Report is to clarify the CBE phenomena, present failure cases where CBE has been the main ESD stress scenario, and collect the existing knowledge for further development of ESD protection methods.

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ESD Association Technical Report for the Protection of Electrostatic Discharge Susceptible Items – Charged Board Event (CBE)**1.0 INTRODUCTION**

In reviewing existing publications, such as ESDA White Paper 2 by Olney and Henry [1] as well as publications by Frank [2], McFarland [3], and Thompson [4], it was found that only anecdotal evidence existed up to 1983 for ESD failures of integrated circuits (ICs) mounted on printed circuit boards (PCBs). These failures had occurred after improperly grounded personnel handled the IC-populated PCBs during the many stages of manufacturing up to and including actual placement in the completed electronic equipment/system. Between 1984 [4] and 1987 [5], it was reported that most components which reportedly failed for the ESD transients on the printed circuit board (PCB), had failed functional testing (that is, the board was inoperable when originally built). Failure analysis (FA), which included de-processing, delayering, and scanning electron microscope (SEM) analysis, of the ICs removed from the PCB, showed that a physical damage showing dielectric or silicon punch-through.

As of 1986, this PCB-related electrostatic discharge (ESD) event was referred to as a “charged board model” (CBM) by Enoch and Shaw [6], and CBM ESD testing was initiated. The measured PCB capacitance (>125 pF) was always much larger than that of the typical 25 pF for the IC devices being built at that time. In 1986, Enoch and Shaw [8], in their study of board-mounted ICs, used the field induced charged device model (CDM) method to charge the board (PCB), then grounded the PCB via one of the input connectors. Koyler et al [5] in 1987 regarded the PCB to be an extended device package but with a much higher capacitance. They suggested two modes by which the board-mounted IC can fail: (i) during the insertion of the device into the board, and (ii) when the PCB discharges into the device, an external to internal mechanism. In 2003 Paasi [9] found board mounted IC failures after they were charged by transportation on conveyor belts. Also in 2003, Olney et al [10] used a standard CDM tester to perform the field-induced stress testing of the components on the PCBs. They modified the boards to fit on the tester table.

Conceptually, the CBM is similar to CDM. During a CDM event, the charge stored by a packaged IC discharges (typically < 100 ps rise time) just before contact is made with a conductive object at or near ground potential. During a CBM event, the charge stored by an entire PCB discharges (similarly, about 100 ps rise time) just before contact is made with a conductive object at or near ground potential. Thus, the named CBM can be thought of as an extension of CDM where the PCB is the “device” that stores the charge. It is suggested that CBM be renamed charged board event (CBE) because CBE does not actually represent a new model, it is just a more severe CDM event. So severe in fact, that the failure can be mistaken for electrical overstress (EOS) damage in some cases. The FA pictures of these CBE failures can be found in later sections as well as in the literature referenced throughout this report.

A usable document that the industry can rely on is needed. The question is: which industries need this? In the working group, the different industrial segments that have been discussed include the PCB, the cell phone, the “board stuffing”, the automotive, and the medical industries. CBE is not as well-known as the classic ESD models but it represents a major real-world ESD threat. Even if all the individual components used for a given PCB have high device or component-level ESD robustness, one or more of these components could be very susceptible to ESD damage after mounting to a PCB since a PCB in general has much higher capacitance [11] than an individual device. CBE damage can be much more severe compared to the CDM damage, therefore, before attributing an extremely severe-looking IC failure on a PCB to other root causes of EOS such as powered handling or AC switching issues.

In 2007, Reinvuo et al [7] modeled the CBE pulses to determine the sensitivity of the electrical components on the board. They argued that the main difference between CDM and CBE is the discharge energy through the component. They discussed and used the physical and essential parameters for the CBE simulation using different sizes of boards (length, width, height, and distance between the charged board and the ground plane of the board). They used and discussed the discharge path parameters (length and point of contact). Their simulations included a