ESD Association Technical Report

ESD TR22.0-02-18

For Relevant ESD Parameters for Seamless ESD Design and Verification Flow – Part 2 – ESD Parameters from Intellectual Property (IP) providers

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ESD Parameters

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FOREWORD

The electronic industry is facing the challenge of the developing highly complex system on chip (SoC) under extreme time and cost pressure. The use of intellectual property (IP) macros of third-party vendors is becoming a widely applied approach to cope with these constraints. Yet, there is in many cases no information, or information that is available is inadequate for determining how to integrate these IP macros into a SoC electrostatic discharge (ESD) top level design. This technical report addresses this demand and describes technical parameters needed, as well as the required communication between IP vendors, SoC design, and foundry. This technical report was published on November 1, 2018 and was designated ESD TR22.0-02-18. At the time ESD TR22.0-02-18 was prepared, the WG22 on ESD Parameters had the following members:

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1.0 Purpose

This document is intended to highlight the ESD-related issues relevant to intellectual property (IP) selection, IP on-chip usage, and IP integration verification. It addresses best practices which are consolidated between IP providers and IP users. Latch-up rules are only addressed as far as they are related to integration of ESD protection elements.

2.0 Scope

The document addresses the necessary interaction between IP design with top level design, foundries, and electronic design automation (EDA) vendors. Based on the key parameters and the categorization and applications of typical IP blocks, the essential rules are discussed. Aspects of EDA design system to facilitate integration of IP blocks is addressed, as well as the need for ESD characterization data.

3.0 Introduction

This document focuses on the ESD communication of the IP providers (see Figure 1).

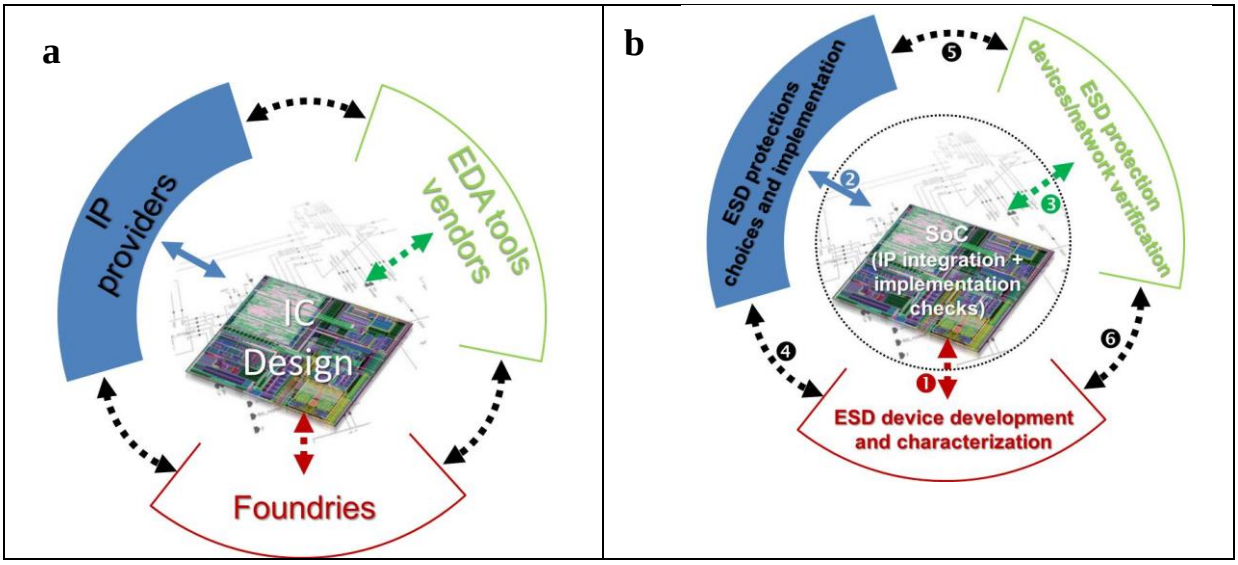

Figure 1: a) Involved Partners (Foundry / IP / EDA Vendor / Integrated Circuit (IC) Design) for ESD Robust IC Design and b) the Typical Activities and Interactions Required for ESD Robust IC Design Between the Various Stakeholders (Foundry / IP / EDA Vendor / IC Design) (see also Table 1)