

AS/NZS 62386.101:2020



Australian/New Zealand Standard™

# Digital addressable lighting interface

**Part 101: General requirements — System components (IEC 62386-101:2014+AMD1:2018 CSV (ED. 2.1) MOD)**



AS/NZS 62386.101:2020

This Joint Australian/New Zealand Standard™ was prepared by Joint Technical Committee EL-041, Lamps and Related Equipment. It was approved on behalf of the Council of Standards Australia on 4 November 2020 and by the New Zealand Standards Approval Board on 4 November 2020.

This Standard was published on 20 November 2020.

The following are represented on Committee EL-041:

- Australian Industry Group
- Better Regulation Division
- CHOICE
- Consumer Electronics Suppliers Association
- Consumers' Federation of Australia
- Department of Industry, Science, Energy and Resources
- Electrical Compliance Testing Association of Australia
- Electrical Regulatory Authorities Council
- Energy Efficiency & Conservation Authority of New Zealand
- IES: The Lighting Society
- Joint Accreditation System of Australia and New Zealand
- Joint Accreditation System of Australia and New Zealand — New Zealand
- Lighting Council Australia
- Lighting Council New Zealand
- Master Electricians Australia
- Master Electricians NZ
- WorkSafe New Zealand

This Standard was issued in draft form for comment as DR AS/NZS 62386.101:2020.

### **Keeping Standards up-to-date**

Ensure you have the latest versions of our publications and keep up-to-date about Amendments, Rulings, Withdrawals, and new projects by visiting:

[www.standards.org.au](http://www.standards.org.au)

[www.standards.govt.nz](http://www.standards.govt.nz)

ISBN 978 1 76113 059 5

Australian/New Zealand Standard™

# Digital addressable lighting interface

**Part 101: General requirements — System  
components (IEC 62386-101:2014+AMD1:2018  
CSV (ED. 2.1) MOD)**

First published as AS/NZS 62386.101:2020.



© IEC 2020 — All rights reserved

© Standards Australia Limited/the Crown in right of New Zealand, administered by the New Zealand Standards Executive 2020

All rights are reserved. No part of this work may be reproduced or copied in any form or by any means, electronic or mechanical, including photocopying, without the written permission of the publisher, unless otherwise permitted under the Copyright Act 1968 (Cth) or the Copyright Act 1994 (New Zealand).

## Preface

This Standard was prepared by the Joint Standards Australia/Standards New Zealand Committee EL-041, Lamps and Related Equipment.

The objective of this document is to specify system components in a bus system for control by digital signals of electronic lighting equipment with the addition of DC supplies.

Tests in this document are type tests. Requirements for testing individual bus units during production are not included.

This document is an adoption with national modifications, and has been reproduced from, IEC 62386-101:2014+AMD1:2018 CSV (ED. 2.1), *Digital addressable lighting interface — Part 101: General requirements — System components*. The modifications are additional requirements and are set out in [Appendix ZZ](#), which has been added at the end of the source text.

[Appendix ZZ](#) lists the variations to IEC 62386-101:2014+AMD1:2018 CSV (ED. 2.1), for the application of this document in Australia and New Zealand.

As this document has been reproduced from an International Standard, the following applies:

- (a) In the source text “this part of IEC 62386” should read “this document”.
- (b) A full point substitutes for a comma when referring to a decimal marker.

Australian or Australian/New Zealand Standards that are identical adoptions of international normative references may be used interchangeably. Refer to the online catalogue for information on specific Standards.

The terms “normative” and “informative” are used in Standards to define the application of the appendices or annexes to which they apply. A “normative” appendix or annex is an integral part of a Standard, whereas an “informative” appendix or annex is only for information and guidance.

## NOTES

## CONTENTS

FOREWORD .....	7
INTRODUCTION .....	9
1 Scope .....	10
2 Normative references .....	10
3 Terms and definitions .....	10
4 General .....	15
4.1 Purpose .....	15
4.2 Version number .....	15
4.3 System structure and architecture .....	16
4.4 System information flow .....	16
4.5 Command types .....	17
4.6 Bus units .....	17
4.6.1 Transmitters and receivers in bus units .....	17
4.6.2 Control gear .....	18
4.6.3 Input device .....	18
4.6.4 Single master application controller .....	18
4.6.5 Multi-master application controller .....	19
4.6.6 Sharing an interface .....	19
4.7 Bus power supply and load calculations .....	20
4.7.1 Current demand coverage .....	20
4.7.2 Maximum signal current compliance .....	20
4.7.3 Simplified system calculation .....	20
4.8 Wiring .....	20
4.8.1 Wiring structure .....	20
4.8.2 Wiring specification .....	20
4.9 Insulation .....	21
4.10 Earthing of the bus .....	21
4.11 Power interruptions at bus units .....	21
4.11.1 Different levels of power interruptions .....	21
4.11.2 Short power interruptions of external power supply .....	21
4.11.3 External power cycle .....	22
4.11.4 Short interruptions of bus power supply .....	22
4.11.5 Bus power down .....	22
4.11.6 System start-up timing .....	22
5 Electrical specification .....	24
5.1 General .....	24
5.2 Marking of the interface .....	24
5.3 Capacitors between the interface and earth .....	24
5.4 Signal voltage rating .....	24
5.5 Signal current rating .....	25
5.6 Marking of bus powered bus unit .....	25
5.7 Signal rise time and fall time .....	26
6 Bus power supply .....	27
6.1 General .....	27
6.2 Marking of the bus power supply terminals .....	27
6.3 Capacitors between the interface and earth .....	27

6.4	Voltage rating .....	27
6.5	Current rating.....	28
6.5.1	General current rating.....	28
6.5.2	Single bus power supply current rating .....	28
6.5.3	Integrated bus power supply current rating .....	28
6.5.4	Dynamic behaviour of the bus power supply .....	28
6.6	Bus power supply timing requirements .....	30
6.6.1	Short power supply interruptions.....	30
6.6.2	Short circuit behaviour.....	30
7	Transmission protocol structure .....	31
7.1	General.....	31
7.2.1	Start bit and data bit encoding .....	31
7.2	Bit encoding.....	31
7.2.2	Stop condition encoding .....	31
7.3	Frame description .....	31
7.4	Frame types.....	32
7.4.1	16 bit forward frame.....	32
7.4.2	24 bit forward frame.....	32
7.4.3	Reserved forward frame .....	32
7.4.4	Backward frame.....	32
7.4.5	Proprietary forward frames .....	32
8	Timing .....	33
8.1	Transmitter timing.....	33
8.1.1	Transmitter bit timing .....	33
8.1.2	Transmitter frame sequence timing .....	33
8.2	Receiver timing.....	34
8.2.1	Receiver bit timing.....	34
8.2.2	Receiver bit timing violation .....	35
8.2.3	Receiver frame size violation .....	36
8.2.4	Receiver frame sequence timing.....	36
8.2.5	Reception of backward frames.....	36
8.3	Multi-master transmitter timing.....	37
8.3.1	Multi-master transmitter bit timing.....	37
8.3.2	Multi-master transmitter frame sequence timing.....	37
9	Method of operation.....	38
9.8	Dealing with frames and commands.....	38
9.8.1	General .....	38
9.8.2	Frame received or rejected .....	39
9.8.3	Frame accepted or ignored .....	39
9.8.4	Command accepted or ignored .....	39
9.8.5	Command executed or discarded.....	39
9.1	Collision avoidance, collision detection and collision recovery .....	40
9.1.1	General .....	40
9.1.2	Collision avoidance.....	40
9.1.3	Collision detection .....	40
9.1.4	Collision recovery .....	42
9.2	Transactions .....	43
9.3	Send-twice forward frames and send-twice commands .....	43

9.4	Command iteration.....	44
9.5	Usage of a shared interface .....	44
9.5.1	General .....	44
9.5.2	Backward frames .....	45
9.5.3	Forward frames .....	45
9.6	Use of multiple bus power supplies .....	45
9.7	Command execution .....	45
10	Declaration of variables .....	45
11	Definition of commands .....	46
12	Test procedures .....	46
Annex A (informative)	Background information for systems .....	47
A.1	Wiring information.....	47
A.2	System architectures .....	48
A.2.1	General .....	48
A.2.2	Single master architecture .....	48
A.2.3	Multi-master architecture with one application controller .....	49
A.2.4	Multi-master architecture with more than one application controller .....	50
A.2.5	Multi-master architecture with integrated input device.....	51
A.2.6	Multi-master architecture with integrated input device and power supply.....	52
A.3	Collision detection .....	53
A.4	Timing definition explanations .....	54
A.4.1	General .....	54
A.4.2	Receiver timing.....	54
A.4.3	Transmitter timing.....	54
A.4.4	Grey areas .....	55
A.5	Maximum current consumption calculation explanation .....	55
A.5.1	Single bus power supply .....	55
A.5.2	Multiple bus power supplies .....	56
A.5.3	Redundant bus power supplies .....	57
A.6	Communication layer overview.....	58
A.6.1	General .....	58
A.6.2	Physical layer .....	58
A.6.3	Data link layer .....	58
A.6.4	Network layer .....	58
A.6.5	Transport layer .....	59
A.6.6	Session layer.....	59
A.6.7	Presentation layer .....	59
A.6.8	Application layer.....	59
A.7	Effects on combining version number 1 and version number 2.y devices.....	59
	Bibliography.....	60
	Figure 1 – IEC 62386 graphical overview .....	9
	Figure 2 – System structure example .....	16
	Figure 3 – Communication between bus units (example).....	17
	Figure 4 – Example of a shared interface.....	19
	Figure 5 – Start up timing example .....	23
	Figure 6 – Maximum signal rise and fall time measurements .....	26

Figure 7 – Minimum signal rise and fall time measurements .....	27
Figure 8 – Bus power supply current behaviour .....	29
Figure 9 – Bus power supply voltage behaviour .....	30
Figure 10 – Frame example .....	31
Figure 11 – Bi-phase encoded bits .....	31
Figure 12 – Bit timing example .....	33
Figure 13 – Settling time illustration .....	33
Figure 14 – Receiver timing decision example .....	35
Figure 15 – Collision detection timing decision example .....	42
Figure 16 – Collision recovery example .....	43
Figure 20 – Dealing with frames and commands .....	39
Figure A.1 – Single master architecture example .....	49
Figure A.2 – Multi-master architecture example with one application controller .....	50
Figure A.3 – Multi-master architecture example with two application controllers .....	51
Figure A.4 – Multi-master architecture example with integrated input device .....	52
Figure A.5 – Multi-master architecture example with integrate input device and bus power supply .....	53
Figure A.6 – Collision detection timing diagram .....	54
Figure A.7 – Transmitter and receiver timing illustration .....	55
Figure A.8 – Bus power supply current values .....	56
Figure A.9 – Current demand coverage .....	56
Figure A.10 – Combination of 4 bus power supplies .....	57
Figure A.11 – Redundant bus power supplies .....	57
Table 1 – System components .....	16
Table 2 – Transmitters and receivers in bus units .....	18
Table 3 – Power-interruption timing of external power .....	21
Table 4 – Power-interruption timing of bus power .....	21
Table 5 – Short power interruptions .....	22
Table 6 – Start-up timing .....	23
Table 7 – System voltage levels .....	24
Table 8 – Receiver voltage levels .....	25
Table 9 – Transmitter voltage levels .....	25
Table 10 – Current rating .....	25
Table 11 – Signal rise and fall times .....	26
Table 12 – Bus power supply output voltage .....	28
Table 13 – Bus power supply current rating .....	28
Table 14 – Bus power supply dynamic behaviour .....	29
Table 15 – Short circuit timing behaviour .....	30
Table 16 – Transmitter bit timing .....	33
Table 17 – Transmitter settling time values .....	34
Table 18 – Receiver timing starting at the beginning of a logical bit .....	35
Table 19 – Receiver timing starting at an edge inside of a logical bit .....	35

Table 20 – Receiver settling time values .....	36
Table 21 – Multi-master transmitter bit timing.....	37
Table 22 – Multi-master transmitter settling time values .....	38
Table 23 – Checking a logical bit, starting at an edge at the beginning of the bit.....	41
Table 24 – Checking a logical bit, starting at an edge inside the bit .....	41
Table 25 – Collision recovery timing .....	42
Table 26 – Transmitter command iteration timing .....	44
Table 27 – Receiver command iteration timing.....	44
Table A.1 – Maximum cable length .....	48
Table A.2 – OSI layer model of IEC 62386.....	58
Table A.3 – Effects on combining version number 1 and version number 2.y devices.....	59

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**DIGITAL ADDRESSABLE LIGHTING INTERFACE –****Part 101: General requirements –  
System components**

## FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

**DISCLAIMER**

**This Consolidated version is not an official IEC Standard and has been prepared for user convenience. Only the current versions of the standard and its amendment(s) are to be considered the official documents.**

**This Consolidated version of IEC 62386-101 bears the edition number 2.1. It consists of the second edition (2014-11) [documents 34C/1098/FDIS and 34C/1111/RVD] and its amendment 1 (2018-05) [documents 34/418/CDV and 34/502/RVC]. The technical content is identical to the base edition and its amendment.**

**This Final version does not show where the technical content is modified by amendment 1. A separate Redline version with all changes highlighted is available in this publication.**

International Standard IEC 62386-101 has been prepared by subcommittee 34C: Auxiliaries for lamps, of IEC technical committee 34: Lamps and related equipment.

This second edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) collection of all bus timing requirements defined in IEC 62386-101:2009 and IEC 62386-102:2009 and rework of the timing requirements to facilitate the preparation of a future control devices standard, taking particular account of the requirements for multi-master systems. The 10 % tolerances have been replaced by minimum and maximum timing values;
- b) integration of multi-master timing requirements;
- c) extension of the defined forward frames;
- d) addition of wiring requirements;
- e) improvement of the bus power supply requirements;
- f) improvement of test sequences and description of the test sequences in the form of pseudo code instead of flow charts.

This Part 101 is intended to be used in conjunction with:

- Part 102, which contains general requirements for the relevant product type (control gear), and with the appropriate Part 2xx (particular requirements for control gear);
- Part 103, which contains general requirements for the relevant product type (control devices), and the appropriate Part 3xx (particular requirements for control devices).

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 62386 series, under the general title: *Digital addressable lighting interface*, can be found on the IEC website

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

**IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.**

## INTRODUCTION

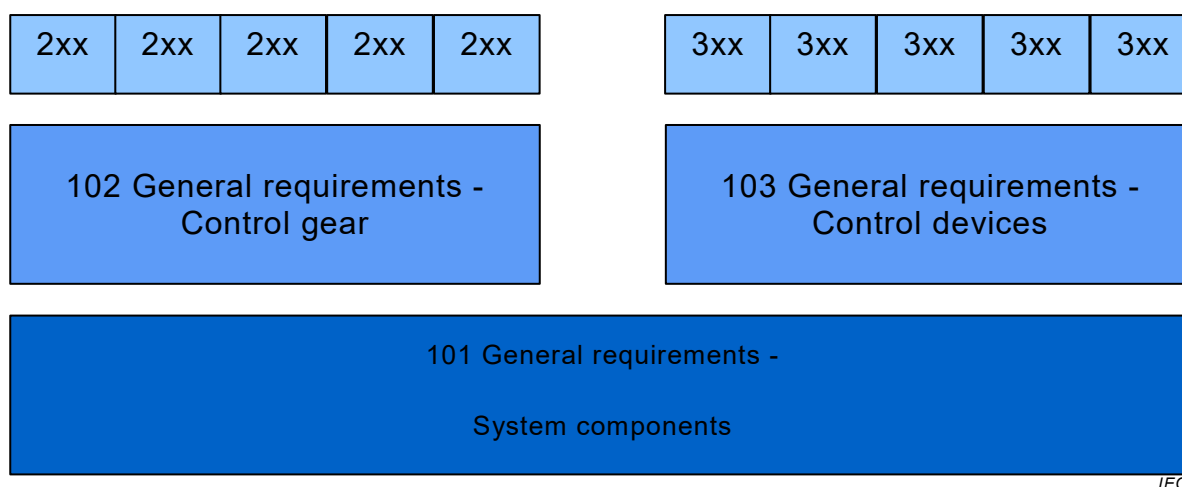
IEC 62386 contains several parts, referred to as series. The 1xx series includes the basic specifications. Part 101 contains general requirements for system components, Part 102 extends this information with general requirements for control gear and Part 103 extends it further with general requirements for control devices.

The 2xx parts extend the general requirements for control gear with lamp specific extensions (mainly for backward compatibility with Edition 1 of IEC 62386) and with control gear specific features.

The 3xx parts extend the general requirements for control devices with input device specific extensions describing the instance types as well as some common features that can be combined with multiple instance types.

This second edition of IEC 62386-101 is intended to be used in conjunction with IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:— and with the various parts that make up the IEC 62386-2xx series for control gear, together with IEC 62386-103:2014 and IEC 62386-103:2014/AMD1:— and the various parts that make up the IEC 62386-3xx series of particular requirements for control devices. The division into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognised.

The setup of the standard is graphically represented in Figure 1 below.



**Figure 1 – IEC 62386 graphical overview**

When this part of IEC 62386 refers to any of the clauses of the other two parts of the IEC 62386-1xx series, the extent to which such a clause is applicable and the order in which the tests are to be performed are specified. The other parts also include additional requirements, as necessary.

All numbers used in this International Standard are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1, "x" in binary numbers means "don't care".

## DIGITAL ADDRESSABLE LIGHTING INTERFACE –

### Part 101: General requirements – System components

#### 1 Scope

This part of IEC 62386 is applicable to system components in a bus system for control by digital signals of electronic lighting equipment which is in line with the requirements of IEC 61347 (all parts), with the addition of DC supplies.

NOTE Tests in this standard are type tests. Requirements for testing individual bus units during production are not included.

#### 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61347-1, *Lamp controlgear – Part 1: General and safety requirements*

IEC 62386-102:2014, *Digital addressable lighting interface – Part 102: General requirements – Control gear*  
IEC 62386-102:2014/AMD1:—<sup>1</sup>

IEC 62386-103:2014, *Digital addressable lighting interface – Part 103: General requirements – Control devices*  
IEC 62386-103:2014/AMD1:—<sup>2</sup>

IEC 61000-4-11, *Electromagnetic compatibility (EMC) – Part 4-11: Testing and measurement techniques – Voltage dips, short interruptions and voltage variations immunity tests*

#### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

##### 3.1

##### **active state**

phase of low level voltage during a transmission

Note 1 to entry: Noise and short pulses may be ignored and therefore do not change the state.

---

<sup>1</sup> Under preparation. Stage at the time of publication: IEC DECFDIS 62386-102/AMD1:2018.

<sup>2</sup> Under preparation. Stage at the time of publication: IEC RFDIS 62386-103/AMD1:2018.