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ESD Association Technical Report

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For

Latch-up Electronic Design Automation (EDA)

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FOREWORD

This technical report[1] was published on February 26, 2021, and was designated ESD TR18.0-02-20. At the time ESD TR18.0-02-20 was prepared, the 18.0 Electronic Design Automation Subcommittee had the following members:

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[1] **ESD Association Technical Report (TR):** A collection of technical data or test results published as an informational reference on a specific material, product, system, or process.

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ESD Association Technical Report for Latch-up Electronic Design Automation (EDA)

1.0 INTRODUCTION

The phenomenon of latch-up has been extensively studied over the past 30 years resulting in the development of different solutions to address latch-up risks [1]. These solutions depend on device operating voltages and process technology, including well isolation techniques. Modern integrated circuits pose additional latch-up challenges due to system on a chip (SoC) complexity: increased metal interconnect resistivity, high device density, and multiple power domains. These challenges have led to the development of latch-up verification techniques relying on electronic design automation (EDA) tools to deliver the coverage necessary to identify and eliminate latch-up risks.

While there is a common understanding of the physical phenomena leading to latch-up across the industry, verification methods to identify these risks vary. This technical report outlines several EDA verification flows and tools used throughout the industry (Section 2.0) to uncover latch-up risks and how future EDA tool development could improve the latch-up verification flow. Section 3.0 gives an overview of scenarios beyond conventional latch-up, including grounded and biased n-wells, transient latch-up, native devices, radiation-induced latch-up, and special high voltage (HV) and FinFET technology requirements. Section 3.0 also includes a description of power management and system-level latch-up challenges, as well as a consideration of triggering parasitic structures during unpowered ESD events. Annex A provides a reference of latch-up prevention design rules classified based on physical category and EDA implementation.

Section 5.0 contains latch-up and EDA term definitions. The latch-up terminology varies within the industry, and where appropriate, other terms are provided.

1.1 Latch-up Overview

Parasitic bipolar devices are inherent in all CMOS technologies. The devices are created when neighboring p and n doped junctions and respective wells, which are part of chip design and manufacturing, interact to form these parasitic devices. Figure 1 shows a cross-sectional view of such a configuration consisting of two parasitic bipolar transistors (npn and pnp) with p-well and n well as the corresponding base terminals of the npn and pnp, respectively. Also, the p-well and n-well act as the collector terminals of the pnp and npn, respectively. Bipolar devices connected in this manner form a pnpn structure, also commonly known as a “thyristor” or silicon-controlled rectifier (“SCR”). Fundamentally, a latch-up event is an unintentional switching of a parasitic thyristor into its “on” state (see Figure 2a).

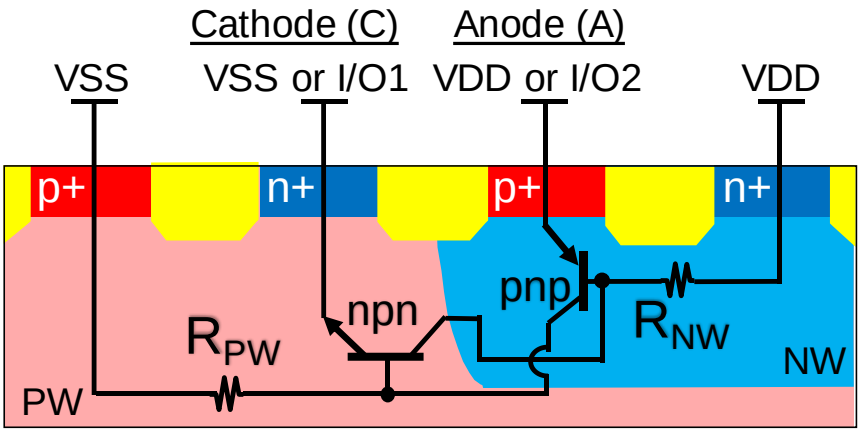

Figure 1: Cross-Section of a Conventional Latch-up Susceptible Structure