ESD Association Standard Practice

ANSI/ESD SP14.5-2021

ANSI/ESD SP14.5-2021

Revision of ANSI/ESD SP14.5-2015

For Electrostatic Discharge Sensitivity Testing

Near-Field Immunity Scanning Component/Module/PCB Level

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard

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ESD Association Standard Practice for Electrostatic Discharge Sensitivity Testing

Near-Field Immunity Scanning Component/Module/PCB Level

Approved January 26, 2021
EOS/ESD Association, Inc.

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FOREWORD

One of the biggest problems when electrostatic discharge (ESD) testing a functional system or subsystem is the analysis of unacceptable soft-errors, upsets, bit errors, and similar faults that occur during ESD testing. These failures are also referred to as “soft” failures, which are non-destructive, and the unit being tested works fine when reset or rebooted. Following a “soft” failure, no physical evidence exists to allow troubleshooting using traditional methods. This standard practice[1] describes a scanning technique for identifying areas, traces, and individual devices that are sensitive to field-coupled transient disturbances. These are likely to be sensitive to the transient electromagnetic disturbances during ESD events or human-metal model ESD testing, as defined by the IEC 61000-4-2 system level ESD test standard. Identifying such areas or devices provides engineers with key information to deduce the causes of “soft” failures, such as upsets and bit errors.

The scanning technique may be performed either under manual control and observation of the device under test (DUT) reactions being monitored by the operator or with a robotic system with automatic failure detection capabilities.

The motivation for using near-field immunity scanning to determine the robustness of components such as integrated circuits (ICs), modules, or printed circuit boards (PCBs) is discussed in the following five points.

Localizing sensitive areas. While the system level standard allows one to determine if a system is passing or failing, it does not identify the root cause of an ESD sensitivity. Root-cause analysis of soft failures is best done with near-field immunity scanning.

Repeatability. The problems of repeatability of system level testing are well-publicized, and near-field scanning has been shown to offer much better reproducibility in determining ESD sensitivities.

Relative characterization at the module level. System level testing requires a complete, operational system, but using near-field scanning allows one to determine individual modules' sensitivity against ESD-like pulses.

Relative characterization at the IC level. Many ESD problems, especially in hand-held products, are not caused by coupling into the PCB but rather by direct coupling into the ICs. Using a near-field scanning system, one can determine an IC's sensitivity to electric or magnetic field coupling.

Fulfillment of system level requirements. Using near-field scanning techniques, one can compare the sensitivities of previous and new models, and in many cases, obtain good indications of robustness without retesting the complete system. This test method is not a substitute for system-level testing but complements it by providing a tool for identifying problem areas.

This document was originally designated ANSI/ESD SP14.5-2015 and approved on August 21, 2015. ANSI/ESD SP14.5-2021 is a revision of ANSI/ESD SP14.5-2015 and approved on January 26, 2021.

[1] **ESD Association Standard Practice (SP):** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it is not reproducible.

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1.0 PURPOSE AND SCOPE

1.1 Purpose

This document establishes a test method for immunity scanning of ICs, modules, and PCBAs. Results from near-field immunity scanning relate to the system level behavior but cannot predict system level performance using the IEC 61000-4-2 test method. The reason is that variations exist in coupling paths between injection points and local current densities and associated fields coupled into traces or ICs.

This test method focuses on soft failures, such as bit errors and upsets, keeping in mind that fast pulses can also cause latch-up. The document will guide the user in identifying the root causes of ESD induced soft failures in components, such as ICs, modules, and PCBAs, for debugging and quality control purposes.

1.2 Scope

This document applies to the testing of powered modules, components such as ICs, circuit boards, subsystems, and systems in which system upset can be detected either by an operator performing the test or automatically.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard practice to the extent specified herein:

ANSI/ESD STM5.5.1, ESD Association Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level[2]

IEC 61000-4-4, Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test[3]

IEC/TR 61967-1-1, Integrated circuits - Measurement of electromagnetic emissions - Part 1-1: General conditions and definitions - Near-field scan data exchange format[3]

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

electrical fast transient (EFT). For this document, an electrical fast transient, as outlined in IEC 61000-4-4 test method, is a burst of electrical events that are coupled onto a system or component.

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[3] International Electrotechnical Commission; 3, rue de Varembé, CH-1211 Geneva 20, Switzerland; www.iec.ch