ESD Association Standard Test Method

ANSI/ESD STM5.5.1-2022

ANSI/ESD STM5.5.1-2022

Revision of ANSI/ESD STM5.5.1-2016

For Electrostatic Discharge Sensitivity Testing

Transmission Line Pulse (TLP) Device Level

EOS/ESD Association, Inc.
218 West Court Street
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An American National Standard
Approved June 9, 2022

Published July 6, 2022

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Approved May 19, 2022
EOS/ESD Association, Inc.

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Published by:

EOS/ESD Association, Inc.
218 West Court Street
Rome, NY 13440

Printed in the United States of America

ISBN: 1-58537-337-0

(This foreword is not part of ESD Association Standard Test Method ANSI/ESD STM5.5.1-2022)

FOREWORD

This document defines a method for pulse testing to evaluate the voltage-current response of the component under test. This technique is known as "transmission line pulse" (TLP) testing. This document simultaneously describes the techniques traditionally known as the standard TLP method (pulse duration in the order of 100 ns), very fast TLP (VF-TLP) method (pulse duration shorter than or equal to 10 ns), and long pulse TLP method (pulse duration more than 200 ns).

TLP testing techniques are used for semiconductor process development, device and circuit design, and failure analysis. This technique or practice is being utilized on products in both wafer level and packaged environments. TLP testing is used as an ESD characterization tool to obtain voltage-current pulse characterization parameters, failure levels, and ESD metrics. The TLP technique is being used today as a standard measurement for ESD devices. The TLP system to the ESD engineer is a tool as critical as the "parameter analyzer" is to the semiconductor engineer. TLP testing is not intended to serve as a technique for ESD qualification of products.

TLP systems are commercially available and can be made by engineers in a laboratory environment. With the use of TLP data for ESD characterization, technology benchmarking, and product quality evaluation, there is a need to have standard testing methodologies and a common means of reporting items such as results, failure criteria, and settings to allow dialogue between semiconductor suppliers, vendors, and product customers.

This document defines the standard test method[1] used in the semiconductor industry for the TLP testing method and techniques in industrial and academic institutions. It also covers the methods used to verify measurement accuracy and to perform system calibration. This document is intended to be used by electrical technicians, electrical engineers, semiconductor process and device engineers, ESD reliability and quality engineers, and circuit designers. The document is intended to delineate a method to be utilized as the TLP standard test method by industry today.

The context of this document is the application of TLP techniques for the electrical characterization of active and passive (semiconductor) components. These semiconductor components can be single devices, a plurality of devices, integrated circuits, or semiconductor chips. This test method applies to diodes, MOSFET devices, bipolar transistors, resistors, capacitors, inductors, contacts, vias, wire interconnects, and related components.

This document covers transmission line based systems applying quasi-rectangular pulses with a wide range of pulse widths and rise times. All are referred to as TLP systems. Further sub-division is discussed in the document. This document can also serve as a basis to describe variants of such systems, for example, non-rectangular pulses or systems based on solid-state pulsers or source measurement units. Additional details about specific aspects of the set-up, configuration, or calibration of TLP equipment and information on TLP and TLP data use cases can be found in ESD TR5.5-04 Transmission Line Pulse (TLP) – User and Application Guide.

This document is focused on the quasi-static behavior of the device under test (DUT). However, many semiconductor devices show peculiar physical effects when stressed by the fast-rising edge of the TLP voltage/current waveform. The analysis of the initial transient phase and characterization techniques are reported in ESD TR5.5-05 Transmission Line Pulse (TLP) – Transient Response Evaluation.

[1] **ESD Association Standard Test Method (STM):** A definitive procedure for the identification, measurement, and evaluation of one or more qualities, characteristics, or properties of a material, product, system, or process that yields reproducible test results.

This document was originally designated ANSI/ESD SP5.5.1-2004 and approved on February 22, 2004. ANSI/ESD STM5.5.1-2008 was a revision and re-designation of ANSI/ESD SP5.5.1-2004 and was approved on February 24, 2008. ANSI/ESD STM5.5.1-2014 was a revision of ANSI/ESD STM5.5.1-2008 and was approved on August 26, 2014. The additional document being merged was designated ANSI/ESD SP5.5.2-2007 and was approved September 16, 2007. ANSI/ESD STM5.5.1-2016 was a revision, consolidation, and re-designation of ANSI/ESD STM5.5.1-2014 and ANSI/ESD SP5.5.2-2007; and was approved on November 2, 2016. ANSI/ESD STM5.5.1-2022 is a revision of ANSI/ESD STM5.5.1-2016 and was approved on May 19, 2022.

Table 1. History of Documents Leading to this Release

Document	Focus	Transition
ANSI/ESD SP5.5.1-2004	100 ns TLP	Original
ANSI/ESD SP5.5.2-2007	VF-TLP	Original
ANSI/ESD STM5.5.1-2008	100 ns TLP	Revision and re-designation of ANSI/ESD SP5.5.1-2004
ANSI/ESD STM5.5.1-2014	100 ns TLP	Revision of ANSI/ESD STM5.5.1-2008
ANSI/ESD STM5.5.1-2016	General TLP	Revision, consolidation, and redesignation of ANSI/ESD STM5.5.1-2014 and ANSI/ESD SP5.5.2-2007
ANSI/ESD STM5.5.1-202x	General TLP	Revision of ANSI/ESD STM5.5.1-2016

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1.0 PURPOSE, SCOPE, AND APPLICATION

1.1 Purpose

The purpose of the document is to establish a methodology for both testing and reporting information associated with transmission line pulse (TLP) testing. This document covers TLP systems applying quasi-rectangular pulses with a wide range of pulse widths and rise times. All such systems are referred to as TLP systems.

1.2 Scope

The scope and focus of this document pertain to TLP testing techniques of active and passive (semiconductor) components. The focus of the document is on the quasi-static application of TLP testing techniques. However, the techniques can also be applied to study the transient behavior of such components.

1.3 Application

Consistent with the definitions in this document, the term Very Fast TLP (VF-TLP) is used for short pulses (≤ 10 ns), the term standard TLP is used for pulses with duration longer than 10 ns and shorter or equal to 200 ns and the term long pulse TLP is used for pulses longer than 200 ns. For long pulse TLP often special considerations need to be taken due to the pulse length.

To indicate a TLP setup with a specific pulse duration, terminology like 100 ns-TLP (for TLP using 100 ns pulses); 1 ns-TLP (for TLP using 1 ns pulses), etc. is used.

Therefore, previous versions of ANSI/ESD STM5.5.1 (2014 and older) typically dealt with 100 ns-TLP, while ANSI/ESD SP5.5.2 (VF-TLP) dealt with TLP systems ranging from 1 ns-TLP to 10 ns-TLP.

The requirements for the equipment and procedures described in this document have been demonstrated to produce repeatable results for quasi-static TLP on different structures in different labs. The results were published in ESD TR5.5-02 and ESD TR5.5-03.

For specific applications and/or practical reasons, useful results may be achieved with parts of the equipment not fully meeting these requirements. If such results are reported, the limitations of the equipment used need to be documented, and the results are not compliant with this document.

NOTE: See ESD TR5.5-04 for more details on possible use cases of TLP and TLP data.

2.0 REFERENCED DOCUMENTS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0, ESD Association Glossary of Terms[2]

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)[2]

IEC 61340-5-1 – Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General Requirements[3]

JESD625 – Requirements for handling Electrostatic-Discharge-Sensitive (ESDS) Devices[4]

[2] EOS/ESD Association, Inc. 218 West Court Street, Rome, NY 13440, Ph: 315-339-6937; www.esda.org

[3] IEC – International Electrotechnical Commission, www.iec.ch

[4] JEDEC, 3103 North 10th Street, Arlington, VA 22201; Ph: 703-907-7534; www.jedec.org