ESDA/JEDEC Joint Standard

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For Electrostatic Discharge Sensitivity Testing

Charged Device Model (CDM) Device Level

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Charged Device Model (CDM) Device Level

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(This foreword is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

FOREWORD

This joint standard[1] was developed under the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a joint working group composed of both ESDA and JEDEC.

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM, a device itself becomes charged (for example, by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. Similarly, a non-charged device can experience CDM stress as a charged conductive object approaches and discharges to the device. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges from other similar scenarios, such as the discharging of charged metal objects to devices at a different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the measuring equipment's limitations and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on many factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage. It has also been shown that the CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package may be less susceptible to CDM damage at a given voltage than that same IC in a package of the same type with a larger area. Section 7.5 and normative Annex C address small package CDM and outlines the procedure to characterize small packages (by technology/common ESD design to those in larger packages, capacitance measurement) such that CDM testing for those small packages may not be needed.

New information includes a procedure to determine multiple level CDM withstand thresholds for subsets of device pins and a more accurate definition of verification module physical characteristics and capacitance measurement/use of modules.

A companion technical report document, ESDA/JEDEC JTR002-01, has also been released to act as a “user guide” for this CDM test standard. The information presented in the user guide is intended to help users better understand the procedures and requirements specified in this standard. References to the user guide are made throughout this standard to aid the reader in the practical elements of adhering to the requirements outlined in this document.

This standard is maintained and revised as a joint standard through a memorandum of understanding between JEDEC and ESDA. This standard is a living document, and revisions and updates will be made on a routine basis driven by the electronic industry's needs.

[1] **EOS/ESD Association, Inc. Standard (S):** A precise statement of a set of requirements to be satisfied by a material, product, system, or process that also specifies the procedures for determining whether each of the requirements is satisfied.

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1.0 SCOPE AND PURPOSE

1.1 Scope

This document establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin-film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. The devices shall be assembled into a package similar to that expected in the final application to perform the tests. This CDM document does not apply to socketed discharge model testers.

1.2 Purpose

The purpose (objective) of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices[3]

JESD88, Dictionary of Terms for Solid-State Technology[3]

JESD625, Requirements for Handling Electrostatic Discharge-Sensitive (ESDS) Devices[3]

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)[2]

IEC 61340-5-1 – Electrostatics – Part 5-1: Protection of Electronic Devices from Electrostatic Phenomena – General Requirements[4]

3.0 DEFINITION OF TERMS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

above-passivation layer (APL). A low-impedance metal plane built on the surface of a die above the passivation layer connecting a group of bumps or pins (typically power or ground).

NOTE: This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

charge time (delay). The amount of time the device is allowed to charge – any additional time is added to the default (set by the manufacturer) in most cases.

charged device model electrostatic discharge (CDM ESD). An ESD stress model that simulates

[2] EOS/ESD Association, Inc., 218 West Court Street, Rome, NY 13440; +1 315-339-6937; www.esda.org

[3] JEDEC Global Standards for the Microelectronics Industry; www.jedec.org

[4] IEC – International Electrotechnical Commission, www.iec.ch