ESDA/JEDEC JTR002-01-22

ESDA/JEDEC Joint Technical Report

ESDA/JEDEC JTR002-01-22

For the User Guide of ANSI/ESDA/JEDEC JS-002

Charged Device Model Testing of Integrated Circuits

Authors:

Joint CDM Working Group

EOS/ESD Association, Inc. and

JEDEC Solid State Technology Association

Electrostatic Discharge Association
218 West Court Street
Rome, NY 13440

JEDEC Solid State Technology Association
3103 North 10th Street
Arlington, VA 22201

Published July 29, 2022

CAUTION NOTICE

Electrostatic Discharge Association (ESDA) and JEDEC Solid State Technology Association (JEDEC) joint standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining the proper product for their particular needs. The existence of such standards and publications shall not in any respect preclude any member or non-member of either Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication that is published by either Association preclude its voluntary use by non-members of such Association whether the document is to be used either domestically or internationally. Recommended standards and publications are adopted by the ESDA and JEDEC in accordance with the ANSI Patent policy.

Interpretation of Joint ESDA/JEDEC Standards: The interpretation of standards in-so-far as it may relate to a specific product or manufacturer is a proper matter for the individual company concerned and cannot be undertaken by any person acting for ESDA or JEDEC. The ESDA Standards Chairman and/or JEDEC Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacturers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard, or on behalf of JEDEC on any JEDEC Standard.

DISCLAIMER OF WARRANTIES

THE CONTENTS OF ESDA'S AND JEDEC'S JOINT STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND NEITHER ESDA NOR JEDEC MAKES ANY REPRESENTATIONS OR WARRANTIES, EXPRESS OR IMPLIED, OF ANY KIND WITH RESPECT TO SUCH CONTENTS. ESDA AND JEDEC DISCLAIM ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, AND NON-INFRINGEMENT.

DISCLAIMER OF GUARANTY

ESDA AND JEDEC'S JOINT STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLER'S OR USER'S OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND NEITHER ESDA NOR JEDEC UNDERTAKES TO GUARANTEE THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURER'S PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA AND JEDEC EXPRESSLY DISCLAIM ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

LIMITATION ON LIABILITY

NEITHER ESDA, JEDEC, NOR THEIR RESPECTIVE PRESENT OR FORMER MEMBERS, OFFICERS, EMPLOYEES OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF, OR IN CONNECTION WITH, THE USE OR MISUSE OF ESDA AND JEDEC JOINT STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING WITHOUT LIMITATION, LOSS OF DATA, INCOME OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY AND CLAIMS OF THIRD PARTIES.

Published by:

Electrostatic Discharge Association
218 West Court Street
Rome, NY 13440

JEDEC Solid State Technology Association
3103 North 10th Street
Arlington, VA 22201

Copyright © 2022 by EOS/ESD Association, Inc. and JEDEC Solid State Technology Association
All rights reserved

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Printed in the United States of America

(This foreword is not part of ESDA/JEDEC Joint Technical Report ESDA/JEDEC JTR002-01-22)

FOREWORD

This technical report[1] is intended to be a complimentary document to ANSI/ESDA/JEDEC JS-002. The intention of this document is to act as a user guide for JS-002 and give the user a wealth of additional information to help them execute CDM testing within their company. This document covers some basic practical considerations such as cleaning and cable replacement and digs into more detailed discussions regarding the oscilloscope and handling charging delays. It also gives a detailed discussion on waveform verification that gives the user a clear/concise approach to completing waveform verification with waveform examples included. This is followed by guidance on the impacts of package size on the peak current, the ability to calculate the charge associated with a waveform discharge, and some practical guidance and ways to handle difficult-to-test packaging that should prove to be very helpful to the user. The final sections address some of the challenges with no-connects, the first pin tested risks, and wraps up with a discussion on reporting CDM data to the customer. The intent is to update this technical report in the future as the joint CDM WG finds new learnings, and each time ANSI/ESDA/JEDEC JS-002 is updated.

This technical report was published on July 29, 2022 and was designated ESDA/JEDEC JTR002-01-22.

[1] **Technical Report (TR):** A collection of technical data or test results published as an informational reference on a specific material, product, system or process.

At the time ESD JTR002-01-22 was prepared, the Joint CDM Subcommittee had the following members:

Alan Righter, Co-Chair Analog Devices		Nathan Jack, Co-Chair Intel Corporation
Troy Anthony Electro-Tech Systems	Robert Ashton Minotaur Labs	Andrea Boroni STMicroelectronics
Brett Carn Intel Corporation	Lorenzo Cerati STMicroelectronics	Mart Coenen EMCMCC
Marcel Dekker MASER Engineering	David Eppes Advanced Micro Devices	Reinhold Gaertner Infineon Technologies
Horst Gieser Fraunhofer EMFT	Evan Grund Grund Technical Solutions, LLC	Fatjon (Toni) Gurga Reliant ESD
Marcos Hernandez Thermo Fisher Scientific	Marty Johnson Texas Instruments (retired)	Chris Jones Semtech Corporation
David Klein pSemi	Peter Koeppen ESD Unlimited	Tim Maloney CAI
Tom Meuse Thermo Fisher Scientific	Kathy Muhonen Qorvo	Paul Ngan NXP Semiconductors
Greg O'Sullivan Micron Semiconductor, Inc.	Nathaniel Peachey Qorvo	Paul Phillips Phasix ESD
Michael Reardon ESDEMC	Masanori Sawada Hanwa Electronic Ind. Co., Ltd.	Marko Simicic imec
Theo Smedes NXP Semiconductors	Wolfgang Stadler Intel Deutschland GmbH	Teruo Suzuki Socionext, Inc.
Peter Turlo ON Semiconductor	Scott Ward Texas Instruments	Terry Welsher Dangelmayer Associates

TABLE OF CONTENTS

1.0 PURPOSE AND SCOPE **1**
1.1 PURPOSE 1
1.2 SCOPE 1
2.0 REFERENCED PUBLICATIONS **1**
3.0 PERSONNEL SAFETY **1**
3.1 TRAINING 1
3.2 PERSONNEL SAFETY 1
4.0 CDM TESTER OPERATIONAL CONSIDERATIONS **2**
4.1 CLEANING 2
4.1.1 Test Cleaning 2
4.1.2 Device Cleaning 2
4.2 ROUTINE VERSUS QUARTERLY CHECKS 2
4.2.1 Tracking Factor/Offset Settings 3
4.2.2 Hardware Changes Requiring Waveform Verification 3
4.3 HOLDING A PACKAGE IN PLACE, Z HEIGHT CAUTION 3
4.4 POGO PIN TIPS (ROUND VERSUS CONCAVE VERSUS SHARP) 5
4.5 HUMIDITY 5
4.6 CABLE CONNECTIONS 5
4.7 1-OHM CURRENT SENSING RESISTANCE MEASUREMENTS 5
5.0 OSCILLOSCOPE EFFECTS - SETTINGS **7**
5.1 METROLOGY CONCERNS 7
5.2 PROPER CABLING AND ATTENUATOR SELECTION 7
5.3 PROPER OSCILLOSCOPE SELECTION 8
5.4 OSCILLOSCOPE VARIATION CONCERNS 8
5.5 PROPER DATA CAPTURE AND ANALYSIS 9
6.0 DETERMINING IF A CHARGE TIME (DELAY) IS NEEDED **9**
6.1 PROCEDURE FOR DETERMINING IF A CHARGE TIME (DELAY) IS NEEDED 9
6.2 PROCEDURE FOR SETTING CHARGE TIME (DELAY) 10
7.0. WAVEFORM VERIFICATION PROCEDURE – FACTOR/OFFSET **11**
7.1 FACTOR/OFFSET ADJUSTMENT METHOD 11
7.2 FACTOR/OFFSET ADJUSTMENT IMPACTS 14
7.3 FACTOR/OFFSET ADJUSTMENT METHOD DETAILS 15
7.3.1 Positive Polarity Waveform Verification 15
7.3.2 Repeat with Negative Polarity 29
8.0 WAVEFORM VERIFICATION PROCEDURE – SOFTWARE VOLTAGE **36**

8.1 SOFTWARE VOLTAGE ADJUSTMENT METHOD 36
8.2 SOFTWARE VOLTAGE ADJUSTMENT METHOD DETAILS 39
8.3 ESTIMATION OF TEST VOLTAGES OTHER THAN THE ANSI/ESDA/JEDEC JS-002 TEST CONDITIONS 49

9.0 PACKAGE VARIABLES AFFECTING FICDM PEAK CURRENT AND PULSE SHAPE ... 50

9.1 THREE-CAPACITOR MODEL 50
9.2 INTERNAL PACKAGE IMPEDANCE AND DIE CIRCUIT EFFECTS 52

10.0 CALCULATION OF CHARGE AND EFFECTIVE CAPACITANCE 53

11.0 SINGLE DISCHARGE VERSUS DUAL DISCHARGE METHOD SELECTION 55

12.0 NO-CONNECT PIN TESTING CONSIDERATIONS 55

12.1 PULSE DETECTION, IP LOGGING, AND EVENT DETECTORS 55
12.2 OVER-STRESS/UNDER-STRESS RISK WHEN ZAPPING NO-CONNECTS 57
12.3 CHOOSING THE CORRECT DISCHARGE METHOD FOR NO-CONNECT PINS 58

13.0 FIRST PIN TESTED WAVEFORM 59

14.0 SMALL PACKAGE PARTS AND CDM 60

14.1 SMALL PACKAGES WITH GULL-WING LEADS 61

15.0 DIFFICULT TO TEST PACKAGES - TIP OVER POTENTIAL 62

15.1 TOXXX PACKAGES 62
15.2 MULTI-WATT PACKAGES 63
15.3 THICK PACKAGES 65
15.4 LONG LEAD PACKAGES 66
15.5 EXPOSED METAL PLATES AND HEAT SINKS 66
15.6 TEST PADS AND PINS DESIGNATED AS NO-CONNECT (NC) OR DO-NOT-USE (DNU) 67

16.0 CDM DATA REPORTING 68

17.0 BIBLIOGRAPHY 68

TABLES

Table 1: Small Verification Module Positive Waveform Summary – Factor/Offset Adjustment Method ... 28
Table 2: Large Verification Module Positive Waveform Summary – Factor/Offset Adjustment Method ... 29
Table 3: Small Verification Module Negative Waveform Summary – Factor/Offset Adjustment Method ... 35
Table 4: Large Verification Module Negative Waveform Summary – Factor/Offset Adjustment Method ... 36
Table 5: Small Verification Module Positive Waveform Summary – Software Voltage Adjustment Method ... 48
Table 6: Large Verification Module Positive Waveform Summary – Software Voltage Adjustment Method ... 48
Table 7: Effect on the Connected Pin Immediately Following a No-connect Pin at High Charge Level ... 58
Table 8: Ip Data for Various Landing Positions of the Pogo ... 66

FIGURES

Figure 1: Relative Position (Z Height or "Cruising Height") of the Pogo Pin to the DUT During the Movement from Pin to Pin During Testing ... 4
Figure 2: A Device Where the Adjustment of the "Cruising Height" Would be Critical to Avoid Hitting the Components in the Center of the Grid During Movement from Pin to Pin ... 4
Figure 3a: Kelvin 4-Wire Resistance Measurement 1-Ohm Current Sensing Resistor Setup ... 6
Figure 3b: Connection of the Kelvin 4-Wire Clips to the 1-Ohm Current Sensing Resistor Setup . 6
Figure 4: Calculated Measurement Accuracy Versus Measurement Current for Different Types of Ohmmeters when Measuring a 1-Ohm Current Sensing Resistor ... 7
Figure 5: Magnitude Response for Gaussian and Maximally-Flat Filters ... 8
Figure 6: Example Characterization of Charge Time (Delay) Versus Ip ... 11
Figure 7: Example Waveform Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method ... 13
Figure 8: Example of the Impact of Factor Adjustment on the Average Ip for the Large Verification Module – High Bandwidth Oscilloscope ... 14
Figure 9: Example of the Impact of Offset Adjustment on the Average Ip for the Large Verification Module – High Bandwidth Oscilloscope ... 15
Figure 10: Example TC 500 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method ... 16
Figure 11: Initial Large Verification Module Reading at TC 500 ... 17
Figure 12: Large Verification Module Reading at TC 500 After Initial Factor Adjustment ... 18
Figure 13: Large Verification Module Reading at TC 500 After Final Factor Adjustment ... 19
Figure 14: Small Verification Module Reading at TC 500 After Final Factor Adjustment ... 20
Figure 15: Example TC 125 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method ... 20
Figure 16: Large Verification Module Reading at TC 125 ... 21
Figure 17: Example TC 250 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method ... 22
Figure 18: Large Verification Module Reading at TC 250 ... 23
Figure 19: Example TC 750 Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method ... 23

Figure 20: Large Verification Module Reading at TC 750 24
Figure 21: Example TC 1000 Verification Flow and Post TC 1000 Checks for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method 25
Figure 22: Large Verification Module Reading at TC 1000 26
Figure 23: Small Verification Module Reading at TC 125 26
Figure 24: Small Verification Module Reading at TC 250 27
Figure 25: Small Verification Module Reading at TC 750 27
Figure 26: Small Verification Module Reading at TC 1000 28
Figure 27: Initial Large Verification Module Reading at Negative TC 500 30
Figure 28: Large Verification Module Reading at Negative TC 500 After Final Factor Adjustment 30
Figure 29: Large Verification Module Reading at Negative TC 125 31
Figure 30: Large Verification Module Reading at Negative TC 250 31
Figure 31: Large Verification Module Reading at Negative TC 750 32
Figure 32: Large Verification Module Reading at Negative TC 1000 32
Figure 33: Small Verification Module Reading at Negative TC 125 33
Figure 34: Small Verification Module Reading at Negative TC 250 33
Figure 35: Small Verification Module Reading at Negative TC 500 34
Figure 36: Small Verification Module Reading at Negative TC 750 34
Figure 37: Small Verification Module Reading at Negative TC 1000 35
Figure 38: Example Waveform Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method 38
Figure 39: Example TC 500 Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method 39
Figure 40: Initial Large Verification Module at TC 500 40
Figure 41: Large Verification Module at TC 500 After Initial Software Voltage Adjustment to 410 Volts 41
Figure 42: Large Verification Module at TC 500 After Final Software Voltage Adjustment of 415 Volts 42
Figure 43: Small Verification Module at TC 500 After Final Software Voltage Adjustment of 415 Volts 42
Figure 44: Example TC 125 Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method 43
Figure 45: Large Verification Module at TC 125 After Final Software Voltage Adjustment of 105 Volts 44
Figure 46: Small Verification Module at TC 125 After Final Software Voltage Adjustment of 105 Volts 44
Figure 47: Large Verification Module at TC 250 After Final Software Voltage Adjustment of 200 Volts 45
Figure 48: Small Verification Module at TC 250 After Final Software Voltage Adjustment of 200 Volts 45
Figure 49: Large Verification Module at TC 750 After Final Software Voltage Adjustment of 615 Volts 46
Figure 50: Small Verification Module at TC 750 After Final Software Voltage Adjustment of 615 Volts 46
Figure 51: Large Verification Module at TC 1000 After Final Software Voltage Adjustment of 815 Volts 47

Figure 52: Small Verification Module at TC 1000 After Final Software Voltage Adjustment of 815 Volts 47
Figure 53: Example Plot of Software Voltage Versus Target Test Voltage Used for the Software Voltage Adjustment Method 49
Figure 54: Illustration of the FICDM Capacitors 50
Figure 55: CDM Peak Current for Package Sizes Up to 2600 mm^2 for 500-Volt Stress 51
Figure 56: Effect of Leaded/Leadless Packages on Peak Current Versus Package Area at 500 Volts 52
Figure 57: Typical CDM Waveform as Measured on a High Bandwidth Oscilloscope 54
Figure 58: Ip Logging on a Larger (52.5 mm x 51 mm) Package Looking at Three Valid IO Pins and Three No-connect Pins at 500 Volts 56
Figure 59: Ip Logging on a Smaller (15 mm x 15 mm) Package Looking at Two Valid IO Pins and Two No-connect Pins at 500 Volts 56
Figure 60: Comparison of Current and Charge of NC pin and Two Subsequent Pins 57
Figure 61: Dual Discharge Event for Connected and No-Connect Pins 59
Figure 62: Examples of Securing a Package Using FR4-Based “Holders” 60
Figure 63: Impact of Template Holders on CDM Ip 61
Figure 64: Examples of SOT23 With and Without Placement on Vacuum Hole 62
Figure 65: Examples of SC70 With and Without Placement on Vacuum Hole 62
Figure 66: Examples of Holding a Package in Place with Risk of Tipping 62
Figure 67: TOxxx Package 63
Figure 68: Ip Versus Charging Voltage of TOxxx Package – Tab Up Versus Down 63
Figure 69: Multi-Watt Package 64
Figure 70: Bending Package Leads to Alter the Pin Height 64
Figure 71: Pogo Pin Landing on Adjusted Lead 65
Figure 72: Adjusting Leads Back to Original Height on ESD Mat 65
Figure 73: Thick Package Limiting Pogo Pin from Landing on Lead 66
Figure 74: TO220 Package Depicting Pogo Landing Locations 66
Figure 75: Examples of Product with an Exposed Metal Plate/Heat Sink 67
Figure 76: Examples of Product with Pin/Balls Removed to Avoid Customer Use 68

ESDA/JEDEC Joint Technical Report for the User Guide of ANSI/ESDA/JEDEC JS-002 – Charged Device Model Testing of Integrated Circuits

1.0 PURPOSE AND SCOPE

1.1 Purpose

The information and procedures defined in this technical report are intended to help users better understand the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

1.2 Scope

This report only covers the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

ANSI/ESDA/JEDEC JS-002, For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) Device Level[2,3]

3.0 PERSONNEL SAFETY

THE EQUIPMENT SHALL NOT BE INSTALLED OR OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

3.1 Training

ALL PERSONNEL SHOULD RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING BEFORE USING THE EQUIPMENT.

3.2 Personnel Safety

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE: CDM TESTERS HAVE MOVING PARTS WHEN IN OPERATION AND CARE SHOULD BE TAKEN TO AVOID PERSONNEL CONTACT WITH MOVING PARTS WHEN IN OPERATION.

[2] EOS/ESD Association, Inc., 218 West Court Street, Rome, NY 13440; +1 315-339-6937; www.esda.org

[3] JEDEC Solid State Technology Association, 3103 North 10th Street, Arlington, VA 22201, www.jedec.org